Following the introduction of 3.0-micron devices (64-Kb DRAMs) in 1975, 2.0-micron devices (256-Kb DRAMs) in 1980 and 1.2-micron devices (1-Mb DRAMs) in 1985, we have now entered the age of submicron devices (4-Mb, 16-Mb and 256-Mb DRAMs). A 1-Gb DRAM is now under development and is scheduled for full production in the year 2000, making designed-in quality and reliability more important than ever.

To meet today's needs, Toshiba has established target quality and reliability levels for verifying reliability in the following areas:

(1) Newly developed process and design rules

(2) New packages

(3) Products

This is done at each phase of the product development cycle. Furthermore, the reliability levels of mass produced products are monitored periodically so as to verify that the predefined reliability levels have been achieved. Failures during these verification processes are analyzed and the failure mechanism for each failure is clarified in order to improve the process. This chapter describes the concept of reliability, the factors affecting reliability, failure mechanisms and analysis examples.

1. Basic Concepts in Reliability Design

1.1 Defining and Quantifying Reliability

Since the beginning of industrial production, companies have strived to improve reliability from the standpoints of durability, product life, safety and serviceability. It is only since 1950, however, that a systematic approach to reliability has been taken. The increasing complexity of machinery, chemical plants and electrical systems has increased dangers to society and increased the importance of reliability as a quality characteristic. This has led to interest in more quantitative methods for defining the concept of reliability with a view to controlling and improving product quality. According to the Japanese Industrial Standards (JIS), reliability is defined as "the probability that an item will perform a required function under specified conditions for a specified period of time."

It is important to note that reliability, as the characteristic of a product, is expressed as a probability which includes three independent concepts: *1* time; *2* spatial factors, such as operating and environmental conditions; and *3* rules for determining whether or not the product performs as specified (the definition of failure).

1.2 Reliability and Time

Of the above-mentioned items, spatial conditions and the definition of failure for each product are constant. Time is the only factor that changes for every device. Therefore, reliability can be defined as a function of time (t).

Reliability concerns the normal functioning of a product over time, whereas quality concerns the normal functioning of a product when it is first operated (at time 0).

Reliability is expressed as a probability value. Depending on how the product is used, the following equations, with time as a variable, can be used to calculate product reliability.

(1) Reliability (or Reliability Function) R(t) (Reliability Function)
This is the ratio of non-defective units after t hours of use to the total number of units at the start of use, i.e. the product survival rate. It is expressed as:

$$R(t) = \frac{No - C(t)}{No}$$

where N_O = Number of non-defective units at the start of usage
$C(t)$ = Number of units that have failed by time t

(2) Non-reliability F(t) (Cumulative Failure Distribution)
This equation calculates the Cumulative Failure Rate from the beginning of use to time t. Its distribution complements that of the Reliability Function R(t), as shown in Figure 1.1.

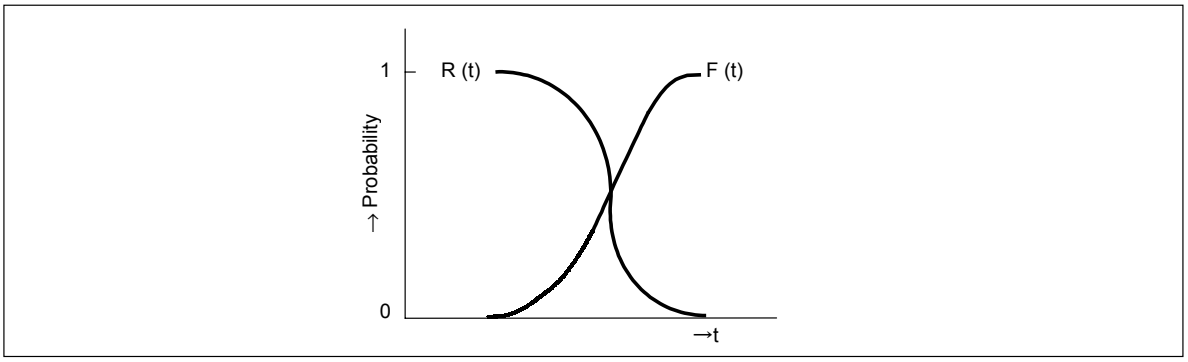


Figure 1.1 Relationship between reliability and cumulative failure distributions

$$F(t) = \frac{C(t)}{No} = 1 - R(t)$$

(3) Failure Density Function $f(t)$
This is the differential of the cumulative failure rate with respect to time. It shows the rate of change in failure at time t.

$$f(t) = \frac{dF(t)}{dt} = -\frac{dR(t)}{dt}$$

The reliability and cumulative failure distribution can be expressed respectively in terms of $f(t)$ as follows:

$$R(t) = \int_t^\infty f(t)dt$$

$$F(t) = \int_0^t f(t)dt$$

(4) (Instantaneous) Failure Rate (or Hazard Rate) $\lambda(t)$
This represents the rate of failure per unit time at time t.

$$\lambda(t) = \frac{f(t)}{R(t)} = -\frac{dR(t)}{dt} \bullet \frac{1}{R(t)} = -\frac{d\ln R(t)}{dt}$$

Reliability can be expressed in terms of $\lambda(t)$ as:

$$R(t) = \exp\left(-\int_0^t \lambda(t)dt\right)$$

According to the MIL standard, failure rate is expressed as "% per 1000h" using 1000h as the unit of time. For semiconductor products, however, it is expressed using the unit FIT.
1 FIT = 10^{-9} (failures/hour) = 10^{-4} (% per 1000h). This is used because the failure rate is very low.

The failure rate of electronic parts generally exhibits uniform behavior, as indicated in Figure 1.2. This is referred to as the "bathtub curve." The bathtub curve can be divided into an initial failure period, a random failure period and a wear-out failure period. Devices subject to failure in the initial period can be found quickly using a process known as "burn-in" (also called "aging," or "heat run"). Such devices can be eliminated before the product ships. Device failure in the wear-out period cannot be eliminated before the product ships, but can be minimized through preventive maintenance. Random failures, however, cannot be foreseen; thus, a primary objective when ensuring reliability is to minimize the failure rate during the random failure period.

It can be observed from past experience that semiconductor devices undergo a gradual decrease in failure rate during the random failure period, as shown in Figure 1.2.

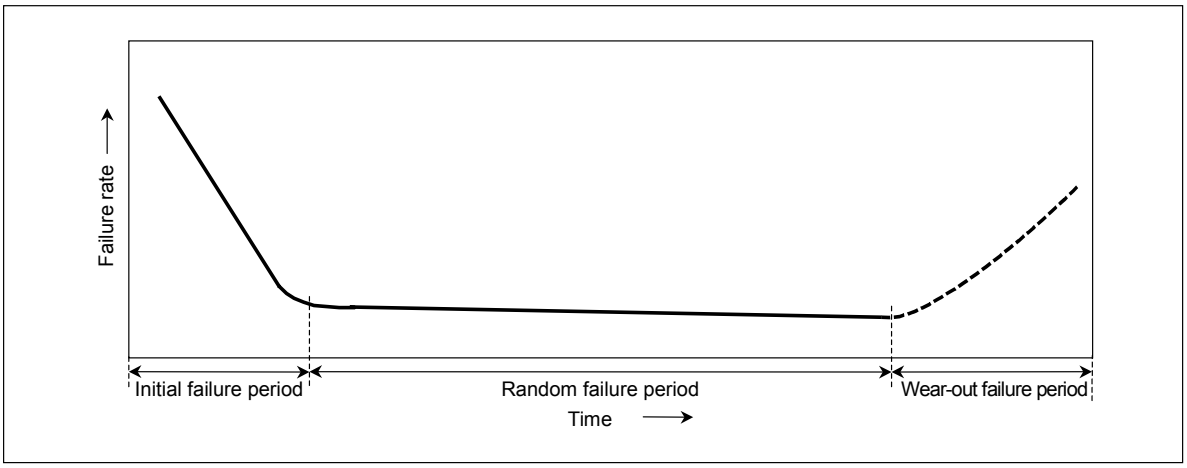


Figure 1.2 Change in semiconductor failure rate over time

(5) Lifetime (Life)
Product lifetime can be expressed in many ways. Mean Time To Failure (MTTF) is used with non-repairable products. Mean Time Between Failures (MTBF) (which shows the mean lifetime) and Useful Life (which shows how long the failure rate will remain below a designated value) are used with repairable products.

MTTF, for devices that cannot be repaired, is found as follows:

$$MTTF = \int_0^\infty tf(t)dt$$

1.3 Operating Environment

The reliability of semiconductor products is determined by their ability to withstand external stresses such as electrical loads, ambient environmental conditions and mechanical loads.

To increase reliability, two things should be done:

(1) Design and manufacture products to withstand forces beyond the anticipated external stress levels.

(2) Limit external stress to a level the product can withstand.

External stresses that affect the reliability of semiconductor products are:

- Electrical stresses such as voltage, current, power and surges
- Ambient environmental stresses such as temperature, humidity, gas, dust and radiation
- Mechanical stresses such as vibration and shock during installation and transport

In order to increase reliability, Toshiba semiconductor products are designed to provide a sufficient margin against the external stresses to which semiconductors are normally subjected, such as thermal and mechanical stress. Reducing external stress can further increase the reliability of the equipment in which semiconductors are used.

For details concerning external stress and derating methods, refer to the next section, Factors Affecting Reliability.

1.4 Designing against Stress

Design and manufacturing techniques must ensure that devices can withstand applied stresses. It is important to analyze the failure factors and take countermeasures.

The junction surfaces of semiconductor devices are very sensitive. Reliability can be adversely affected by the manufacturing process, circuit layout or wiring for electrical connections. Thus, semiconductor design (the design of processes, circuits and packages) is very important. During full-scale production, manufacturing processes are subjected to strict process QC and screening controls. Various reliability tests and marketing analyses determine the deficiencies of a product, and this information is used to take corrective action and implement reliability improvements. Due to the rapid progress of semiconductor technology, the failure analysis method has proven best for improving reliability.

This failure analysis is based on the idea that failures occur when external stresses are applied to the device. It is not a new idea.

The method involves comprehensive analysis of failures to determine the inherent deficiencies in a product. This information is then fed back into the design and production processes. The constant flow of information and rapid implementation of improvements allow quick response to market demands for improved semiconductor reliability. This process is detailed in Appendix 2, Mathematics of Reliability.

2. Factors Affecting Reliability

2.1 Design

The design phase of a product is very important to its reliability.

Semiconductor design factors are listed in Table 2.1. The three major design categories are: pattern, manufacturing process and package.

With IC design, the transistor (bipolar or MOS) geometry and other factors that affect performance are determined during the pattern design phase according to the functional characteristics required of the device. Transistors are then connected to obtain the desired functions. During this process, continuous efforts are made to minimize the lengths of the metal interconnections between transistors and the size of individual elements. Nowadays this process is automated with the aid of computers and design is performed according to predefined design rules. The factors in Table 2.2 are incorporated into the design rules and verified by computer.

The manufacturing process is designed to realize the expected characteristics, which are based on the pattern design. It is broadly divided into two processes: (1) wafer fabrication, which puts the transistors, diodes and resistors on the silicon substrate as dictated by the pattern, and (2) the assembly process, consisting of die separation, die bonding, wire bonding and sealing to form the final product structure.

During wafer fabrication, various technologies are used to achieve exactly the right size and shape for the diffusion layer, oxide film and metal interconnections. Continuous efforts are made to maintain consistency in these characteristics. Manufacturing precision is incorporated into the design rules and fed back to pattern design.

Packages are designed to protect components (both mechanically and thermally) on the silicon substrate. There are two major types of package: hermetically sealed, with an internal cavity structure; and plastic-encapsulated, in which the chip is buried in the resin. Materials such as glass, ceramic, metal and resin are used in package construction.

2.2 Manufacturing Process

The semiconductor manufacturing process includes various steps, such as heat treatment, chemical treatment, testing and inspection, which can affect product reliability. Factors that can degrade reliability include problems within the manufacturing process, such as human error and equipment faults. The semiconductor manufacturing process is extremely complicated, requiring great precision. In addition, because product characteristics are extremely sensitive to variations in the manufacturing process and to external conditions, it is essential to fully understand all factors affecting reliability.

Table 2.2 lists factors affecting product reliability which are related to the manufacturing process. The manufacturing process repeats several processes to form the elements of the semiconductor product, such as transistors, resistors and capacitors, which are placed on a silicon substrate and interconnected to form circuits. These processes take place in clean rooms to avoid dust and other contaminants that greatly affect reliability. It is particularly important that the dust level be

controlled precisely at the particle submicron level.

Of the factors listed in Table 2.2, those related to the wafer (silicon substrate) are most fundamental to the product. Factors such as crystal defects in the silicon, resistivity dispersion and contamination surface flaws can directly affect product characteristics.

The assembly process begins with die separation. In this process the most critical operations are die bonding, wire bonding and the sealing or molding processes. Die bonding and wire bonding are the processes that mount the die and bond wires which are used to connect the external package leads to the chip. Since junctions are formed between different materials, changes in temperature and other physical forces (such as vibration, shock and acceleration) can cause the die to crack or cause open faults, either of which can be catastrophic. In the case of resin molding, impurities in the molding resin (such as sodium, potassium or chlorine), absorption of moisture, thermal expansion and mold shrinkage must be taken into account. These can result in corrosion failure, improper characteristics, breakage of bonding wires and die cracks. In the case of hermetic sealing, checks must be carried out for moisture and other impurities in the sealing gas and the presence of conductive material. These can cling to the die surface and cause increased leakage current or improper operation.

2.3 Operating Environment

2.3.1 Environmental Conditions

Internal product factors affecting reliability can be accelerated by external stresses, such as the operating environment. Typical external factors are listed in Table 2.3.

Some factors operate independently. Generally, however, external factors affecting reliability are interrelated. For example, corrosion breakage is caused by a combination of temperature and humidity.

Stresses are classified into those deriving from the natural environment and those related to human factors. Stresses deriving from the natural environment include temperature, humidity, atmospheric pressure, salinity, overvoltage surges due to lightning and cosmic rays. Temperature and humidity are the most significant factors.

In general, a rise in temperature speeds up chemical reactions and accelerates changes in materials. This in turn accelerates failure mechanisms. Therefore, temperature must be monitored carefully. When the product is operating, increase in temperature due to power dissipation by the device must also be taken into account.

Change in temperature stresses the junction between two different materials when the materials expand at different rates. If this occurs repeatedly, material fatigue in the junction can damage the hermetic seal and degrade die bond adhesion, causing bonding wire opens. If the device is connected improperly, heat from the equipment or the device can accelerate the temperature change, thus accelerating the fatiguing process.

Humidity-induced condensation increases the conductivity of material surfaces. This increases leakage current in a device, which in turn affects the characteristics and functions of the device. Humidity can also accelerate chemical and electrochemical reactions which cause metal corrosion.

Resin-encapsulated devices are especially susceptible to humidity. However, due to improvements in resin materials, resin molding is now by no means inferior to hermetic sealing.

Atmospheric pressure affects devices used at high altitudes, e.g. in mountainous areas or in aerospace applications. Low atmospheric pressure induces a corona discharge between electrodes and reduces the package's heat radiation rate. This results in a temperature rise in the die.

Salinity is a problem for devices used in coastal areas, ships and other marine applications. Salt adhering to device surfaces increases the chance of metal corrosion damage and diminishes the insulation between electrodes.

Lightning can affect devices in outdoor applications, such as traffic signaling equipment. Special protective measures should be taken to increase the ability of devices to withstand voltage surges caused by lightning.

Other natural environmental factors include soft errors due to alpha rays from radioactive isotopes in packaging materials (this normally affects high-integration LSI memory), and damage or malfunction due to radiation inherent in certain applications, such as nuclear power and aerospace.

Human factors affecting reliability include the subjection of devices to vibration during transport and in vehicular applications (Table 2.4); shock during handling by industrial robots or caused by dropping, impact, etc. during device operation (Table 2.5); overheating during printed circuit board soldering; voltage surges during the opening and closing of switches; noise from poor relay contacts or nearby electric motors; electrostatic problems in low humidity environments; malfunctions due to strong electromagnetic waves from a nearby transmitter or oscillator; and ultrasonic vibration during printed circuit board cleaning after soldering.

2.3.2 Operating Conditions

In addition to physically induced stress caused by the natural environment and human error, operating conditions imposed by the equipment or system in which a semiconductor is used can also affect reliability. Examples are device breakdown due to operation at higher-than-rated-for voltages; malfunction due to operation at lower-than-rated-for voltages; destruction due to excessive loads; and malfunction or destruction when device timing specifications are not adhered to.

2.4 Factor Analysis Techniques

In general, the analysis of reliability factors during product design and process design is very effective for improving reliability. The main reliability factor analysis techniques are:

(1) Design Review (DR)

(2) Fault Tree Analysis (FTA)

(3) Failure Mode and Effect Analysis (FMEA)

DR, in the case of semiconductor devices, means verifying the items shown in Table 2.1 and correcting any problems so as to yield a more robust product. Normally, a design standard is defined to simplify and guide this process. Design thus proceeds according to the standard and the design is checked against the standard during the DR. If there are any deviations, tests are run to confirm adherence to the standard and the standard is updated as necessary.

FTA analyzes factors contributing to device failure, such as circuit configuration, pattern design, manufacturing process, package design and operation method.

The analysis divides the design, manufacturing, packaging and operation phases into well-defined detailed functional items. The possible failure modes and the effects of such failures are known for each item. These items are then weighted so that countermeasure priorities can be defined and established.

An example of the FMEA method is shown in Table 2.6 for a plastic-package MOS LSI manufacturing process. Using a scale of 1 to 10, the Failure Index section of the table rates failure information in terms of frequency, effect (on the product, equipment or system) and detectability. A failure index is calculated by multiplying these three rated values together. The larger the index value, the more serious the failure.

The last column in Table 2.6 shows countermeasures for each process-related failure.

Table 2.1 Design factors affecting reliability (1/2)

Design item		Related Factors	Failure Mode
Pattern design	Transistor (bipolar)	Size and shape (collector, base, emitter), doping impurity concentration, diffusion depth	Functional failure
	Transistor (MOS)	Size and shape (W/L), oxide film thickness	Functional failure
	Isolation	Width, diffusion depth, doping impurity concentration	Parasitic transistor, leakage current, insufficient breakdown voltage
	Resistance (diffusion)	Size and shape, diffusion depth, doping impurity concentration	Functional failure, insufficient breakdown voltage, short
	Resistance (polysilicon)	Size and shape, doping impurity concentration, film thickness	Functional failure, open
	Metallization (aluminum)	Size and shape, film thickness	Electromigration, open, short
	Metallization (polysilicon)	Size and shape, film thickness, doping impurity concentration	Functional failure, open
	Metallization contact with silicon	Size and shape, contact combination (e.g. Al-silicon, Al-polysilicon)	Open, short (alloy spike)
	Bonding pad	Size and shape, wiring lead shape	Improper bonding, open
	Bonding pad layout	Bonding pad distance, package, relative bonding positions	Bonding wire open/short, bonding wire displacement (resin mold)
	I/O protection circuit	Protective resistance, protective diode/transistor	Electrostatic discharge, surge damage
Manufacturing process design	Photoengraving process (PEP) Photoresist application	Film thickness, dust, foreign particles, photoresist material	Improper pattern geometry (open, short, characteristic failure), pinhole
	Photoengraving process (PEP) Mask alignment	Accuracy of alignment	Characteristic failure
	Photoengraving process (PEP) Exposure	Time, intensity of illumination	Improper pattern geometry (open, short, characteristic failure)
	Photoengraving process (PEP) Development	Time, developing solution	Improper pattern geometry (open, short, characteristic failure)
	Photoengraving process (PEP) Etching	Time, temperature, etching solution	Improper pattern geometry (open, short, characteristic failure)
	Oxidation (thermal oxidation method)	Temperature, time, reaction gas, film thickness	Functional failure (e.g. V_{th}, h_{fe})
	Passivation deposition (CVD method)	Temperature, time, reaction gas, film thickness	Functional failure(e.g. V_{th}, h_{fe}, leakage)
	Diffusion (thermal diffusion)	Temperature, time, doping impurity concentration, diffusion depth	Functional failure, insufficient breakdown voltage
	Diffusion (ion implantation)	Acceleration voltage, dosage, ion source, implantation depth	Functional failure
	Metal deposition (aluminum)	Deposition method, temperature, film thickness	Functional failure, open, short
	Metal deposition (polysilicon)	Temperature, time, reaction gas, film thickness	Functional failure, open, short
	Die separation	Dicing method, wafer thickness	Die crack, flaw, short
	Die bonding	Die bonding method, temperature, die bonding material (Au-Si, epoxy etc.)	Characteristic failure (unstable action)
	Wire bonding	Wire bonding method (thermal compression, ultrasonic bonding etc.) wire material (Au, Al), wire diameter	Open, short
	Sealing (hermetic sealing)	Sealing method (metal, glass etc.), sealing width	Defective hermetic seal, large leakage current, corrosion breakage
	Encapsulation (resin molding)	Molding method, temperature, time, material characteristics (thermal expansion coefficient, impurities)	Functional failure, die crack, open, short, wire corrosion breakage
	Lead forming	Lead-forming method, size and shape	Broken package, lead shape, abnormality, broken lead
	Lead finishing	Treating method (plating, dipping), protective material (gold, tin, solder etc.)	Rusting, contact fault, solder fault
	Marking	Temperature, time, marking method	Marking erosion, illegibility

Table 2.1 Design factors affecting reliability (2/2)

Design item		Related Factors	Failure Mode
Package design (hermetically sealed)	Sealing method	Glass, metal welding, metal fusion, resin bonding, sealing condition	Hermetic fault, functional fault, large leakage current, corrosion
	Sealing gas	Chemical reaction, moisture content	Functional fault, large leakage current, corrosion
	Package material	Glass, ceramics, metal, resin, thermal expansion, mechanical strength	Broken package, hermetic fault, functional fault, thermal runaway
	Package shape and size	Correlation between die size and package size, size tolerance for sealed part	Insufficient hermetic seal, functional fault
	External lead material	Electrical conductivity, hardness, thermal expansion, corrosion resistance, mechanical strength	Contact fault, lead breakage fault
	External lead shape and size	Lead section shape, tensile strength, bending strength	Broken or defective lead
Package design (resin molding)	Molding method	Transfer mold, bonding etc.	Open, short (bonding wire)
	Molding resin material	Base resin, hardening agent, chemical resistance, impurities, thermal expansion, thermal conductivity	Functional fault, open, short (bonding wire), corrosion
	Package shape and size	Correlation between die size and package size, size tolerance for sealed part	Missing external lead, open, short, corrosion
	Molding condition	Temperature, time, pressure	Open, short (bonding wire), bonding wire displacement
	External lead material	Electrical conductivity, hardness, thermal expansion, corrosion resistance, mechanical strength	Contact fault, lead breakage fault
	External lead (shape and size)	Lead section shape, tensile strength, bending strength	Lead breakage fault

Table 2.2 Manufacturing process factors affecting reliability

Manufacturing Process Affecting Reliability			Related Items on Device	Related Factors	Failure Mode
Wafer process	Wafer (silicon substrate)		Silicon bulk	Resistivity variation, crystal defect, surface dirt, cracks, flaws, warping, distortion	Characteristic fault, unstable operation, short, open
	Oxide film		Field oxide, gate oxide, interlayer insulator, passivation film	Pin holes, cracks, uneven thickness, contamination, step coverage faults	Reversed surface, channel leakage, V_{th} shift, degraded breakdown voltage, h_{FE} shift, noise, unstable operation
	Photoengraving process (PEP)	Resist application	Transistor, diode, resistance, metallization, shape and size, contact	Improper film thickness, uniformity, foreign particles, residual photoresist	Characteristic fault, pin hole, large leakage current
		Mask alignment	Transistor, diode, resistance, metallization, shape and size, contact	Misalignment, dust, foreign particles, flaws	Characteristic fault, pin hole, large leakage current
		Exposing	Transistor, diode, resistance, metallization, shape and size, contact	Insufficient exposure	Characteristic fault
		Development	Transistor, diode, resistance, internal wiring, shape and size, contact	Insufficient developing	Characteristic fault
		Etching	Transistor, diode, resistance, internal wiring, shape and size, contact	Insufficient etching, etching temperature out of range, insufficient washing	Characteristic fault, characteristic fluctuation
	Diffusion (thermal diffusion)		Transistor, diode, diffusion resistance, isolation, contact	Abnormal diffusion (transverse, depth), impurity separation, crystal defects, improper impurity concentration	Characteristic fault, degraded breakdown voltage, open, short, unstable operation
	Diffusion (ion implantation)		Transistor, diode, diffusion resistance, contact	Oxide film, damaged silicon bulk, insufficient dose amount, insufficient implantation depth	Characteristic fault, degraded breakdown voltage, open, short, unstable operation
	Metal deposition (aluminum)		Transistor electrode, internal wiring, contact, MOS gate electrode	Flaws, voids, step coverage, delamination, insufficient thickness, electromigration, doping concentration, contamination	Open, short, increased electrical resistance, corrosion
	Polysilicon deposition		MOS gate electrode, resistance, internal wiring, contact	Flaws, step coverage, delamination, insufficient thickness, doping concentration	Open, short, increased electrical resistance
Assembly process	Die separation		Die periphery	Flaws, cracks, contamination	Characteristic fault, large leakage current, degraded breakdown voltage, corrosion
	Die bonding		Die bonding	Insufficient die adhesion, adhesive debris, degassification (resin bonding)	Characteristic fault, unstable operation, large leakage current, short
	Wire bonding		Bonding wire	Improper bonding pressure, improperly connected bonding wire or bonding wire loop, wire flaws, contamination, deficient wire adhesion	Open, short (package, die), broken wire, peeled bonding
	Sealing (hermetic)		Package	Insufficient sealing, improper sealing gas (moisture, impurities), dirt on surface, presence of foreign matter	Increased leakage current, corrosion breakage, short, intermittent fault
	Encapsulation (resin molding)		Package	Defective molding (cavities, cracks), bonding wire displacement, insufficient lead frame sealing, molding shrinkage distortion, moisture absorption	Bonding wire open/short, corrosion breakage (die, metal wiring), die crack, improper characteristics
	Lead forming		Lead terminal	Improper shape, damage, insufficient terminal strength	Open, improper contact
	Lead finish		Lead terminal	Oxidation, rusting, residual surface treatment solution (insufficient washing)	Open, improper contact, inter-terminal leakage
	Marking		Top surface of package	Illegible mark	Breakage due to inappropriate use

Table 2.3 Operating environment factors affecting reliability

Stress Factor		Where and When It Can Occur	Failure Mode
Temperature	High temperature	Tropics, deserts, space, cars, other special environments	Characteristic fault, unstable operation
	Low temperature	Cold zone, high altitude, space, aircraft, other special environments	Characteristic fault, unstable operation
Temperature change		When operated intermittently	Die crack, degraded die bonding, characteristic fault, unstable operation
Humidity	High humidity	Tropics, tunnels, cars, other special environments	Rusting, improper contact, corrosion, characteristic fault
	Low humidity	Deserts, in low-humidity weather	Electrostatic damage
Atmospheric pressure	Low atmospheric pressure	High altitude, mountainous areas, aircraft	Corona discharge, low heat dissipation, characteristic fault
	Vacuum pressure	Space	Corona discharge, low heat dissipation, characteristic fault
Salinity		Coastal areas, on the sea, ships, marine facilities	Rusting, improper contact, damaged lead
Vibration		During product transportation, vehicle-mounted equipment, machine tools, aircraft equipment	Bonding wire open (hermetic seal), damaged lead (board mounted), package crack
Impact, dropping		During product transportation, vehicle-mounted equipment, machine tools, aircraft equipment	Package crack, deformed lead
Acceleration		Aircraft equipment, rockets, other special-purpose equipment	Bonding wire open (hermetic seal), damaged package
Heating		During assembly process (e.g. soldering)	Characteristic fault, deformed package shape
Electrical overstress, surge		During On/Off operation of switches and relays, capacitive loads, motors	Characteristic fault, short
Noise		Motors, when used with improper contacts	Characteristic fault, short
Electrostatic discharge		When handling in low humidity, near strong field generating equipment, during transportation	Characteristic fault, short
Strong electromagnetic field		Near a transmitter or signal generator	Characteristic fault
Ultrasonic wave		When cleaning circuit boards after soldering	Open bonding wire (hermetic seal), erased marking
Radiation		Nuclear power-related facilities, space (satellite)	Characteristic fault, destruction, soft error
Erroneous operation	Overvoltage	When used with invalid operating supply voltage	Destruction, degraded breakdown voltage, short
	Overload	When used with invalid drive capacity	Destruction, short
	Others	When used at invalid operating timings etc.	Characteristic fault, latch-up

Table 2.4 Environments with excessive vibration

Environment		Shock
Land Transportation	Road	1 Hz~3 Hz at up to 29.4 m/s^2 15 Hz~40 Hz at 9.81 m/s^2
	Rail	14.7 m/s^2 2 Hz~100 Hz with amplitude ± 0.05 mm
Sea		Frequency 1 Hz~50 Hz Amplitude 2.5 mm~0.075 mm
Air		Frequency 3 Hz~500 Hz Amplitude 3 mm~0.025 mm

Table 2.5 Environments with excessive shock

Environment		Shock
Land Transportation	Road	58.9 m/s^2 peak Shock width 5 mm/s~40 mm/s
	Rail	When coupling and decoupling rolling stock 196 m/s^2 Speed change: 5.4 m/s
Sea		——
Air		Shock on arrival and departure of up to 36 m/s^2

Table 2.6 Manufacturing process FMEA example (resin molding)

Process Stage	Failure Mode	Effect of Failure	Cause of Failure	Failure Index				Countermeasures
				Frequency	Effect	Detectability	Index	
(1-10) Al metallization	Improper thickness, voids in metal, metal open	Electromigration, open circuit	Operator mishandling, foreign particles, poor adjustment of equipment	2	9	2	36	Improvement and adjustment of work procedures, dust control, in-process inspection (SEM)
(1-11) Passivation	Lack of passivation film, non-uniform film, thickness	Increased leakage current, characteristic fault	Foreign particles, operator mishandling	2	2	4	16	Dust control, improvement and adjustment of work procedures
(1-12) Visual inspection	Scratch, die crack, contamination, residual photoresist	Open circuit, increased junction leakage current	Mishandling of wafer, erroneous wafer cleaning	2	2	2	8	Improvement and adjustment of work procedures
2 Assembly process (2-1) Die preparation	Die crack	Increased junction leakage current, characteristic fault	Poor adjustment of equipment, operator mishandling	1	3	2	6	Operator training, improvement and adjustment of work procedures
(2-2) Die bonding	Die crack, die floating	Open circuit, increased junction leakage current, characteristic fault	Operator mishandling, temperature decrease	1	9	2	18	Operator training, improvement and adjustment of work procedures, visual inspection
(2-3) Wire bonding	Bonding open, improper bonding position, shorted bonding wire	Open, short	Poor bonding strength, operator mishandling, poor adjustment of equipment, abnormal loop shape	2	10	1	20	Operator training, improvement and adjustment of work procedures, visual inspection
(2-4) Resin molding	Bonding wire open, shorted bonding wire, package crack, corrosion	Open, short, defective appearance	Poor adjustment of equipment, insufficient curing	2	10	2	40	Operator training, improvement and adjustment of work procedures, visual inspection
(2-5) Lead finish (plating)	Insufficient thickness of metal plating, dirt	Poor soldering, improper contact	Operator mishandling, poor adjustment of equipment, insufficient cleaning	1	2	3	6	Improvement and adjustment of work procedures, operator training
(2-6) Lead forming	Abnormal shape, broken lead	Soldering fault, characteristic fault	Operator mishandling, poor adjustment of equipment	1	2	1	2	Improvement and adjustment of work procedures, operator training
(2-7) Marking	Marking error, illegible marking	Breakage	Operator mishandling, insufficient curing	1	1	1	1	Improvement and adjustment of work procedures

3. Failure Mechanisms in Semiconductors

This section describes semiconductor failure mechanisms in terms of fault areas in devices (see the MOS integrated circuit diagram in Figure 3.1). Descriptions of assembly technology failure mechanisms refer primarily to Figure 3.2.

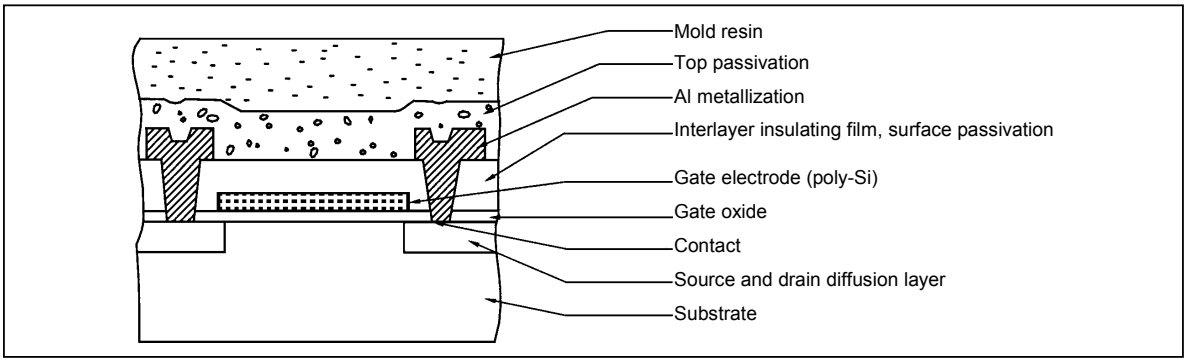


Figure 3.1 Schematic diagram of MOS integrated circuit chip

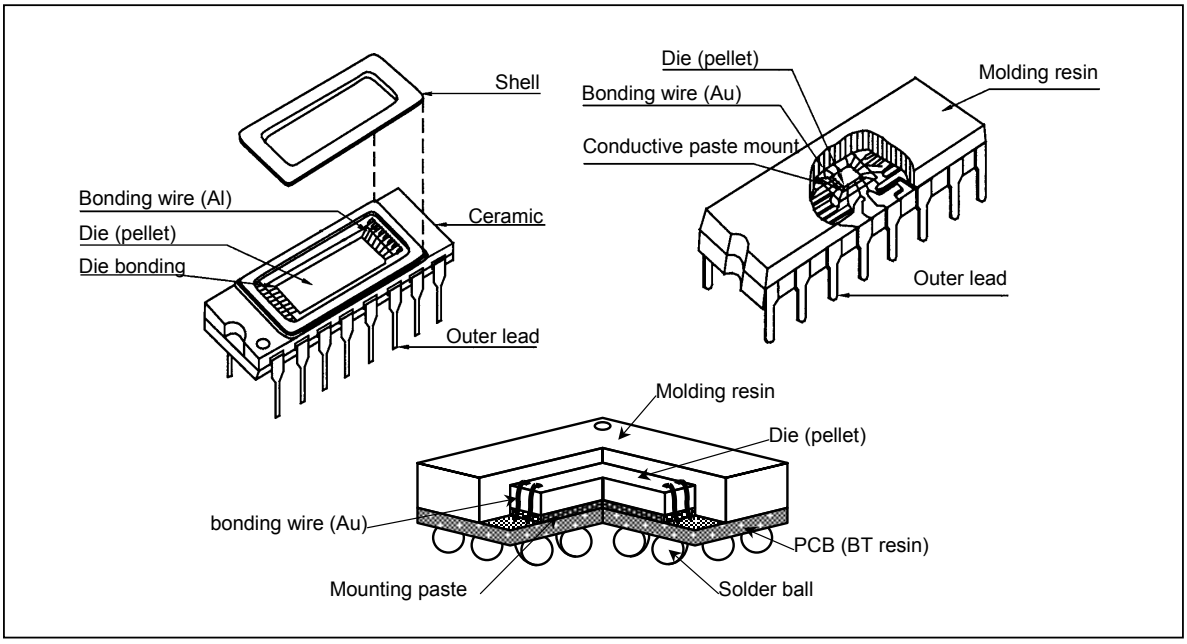


Figure 3.2 Structure of a semiconductor device

3.1 Substrates

Materials used for semiconductor substrates include Si single-crystal, Si epitaxial, GaAs and GaP. Advances in crystal processing technology have made the manufacture of dislocation-free Si single-crystal possible. Currently, attention is being paid to defects occurring during the oxidation and diffusion processes, distortion and micro-cracks which occur during the crystal-forming process, and stacking faults known as OSFs (oxidation-induced stacking faults). These types of crystal defect, when dense, increase the reverse current in the PN junction, degrading the retention time in DRAM and causing a leakage current in SRAM. In bipolar devices these defects degrade the breakdown voltage[1)] characteristics and reduce h_{FE}. Countermeasures include oxygen density control in the crystal, optimization of gettering and other processes, and cleaning.

If the resistance in the Si substrate deviates from the desired value, yields and reliability are affected. This is due to a piezo-resistance effect caused by physical stress during resin encapsulation. Countermeasures include encapsulating the device in low-stress resin or incorporating sufficient margin in the design to allow for resistance changes.

3.1.1 PN Junction

With improved pattern designs and product process designs, characteristic faults due to degradation in the PN junction have become negligible. However, recent continuing progress in microscopic processes has increased the possibility of errors due to external stress factors.

One such factor is electrical overstress (EOS). This is caused by an excessive current flow between the power supply and GND when parasitic PNP and NPN transistors turn on due to the nature of the device's structure. This is especially common in CMOS devices and is referred to as the "latch-up" phenomenon. It induces open failures in Al metal interconnections and bonding wires. Countermeasures include lowering the h_{FE} of parasitic transistors and optimizing the pattern design. However, precautions must also be taken regarding the operating conditions. (See Chapter 5.)

Another example of external stress is electrostatic discharge (ESD). When ESD applies a reverse bias to the PN junction, heat due to power dissipation melts the Si, damaging the junction. On-chip protection is normally provided by inserting resistors and protective diodes to disperse the voltage and current.

3.1.2 Alloy Spikes

The primary metallization material for semiconductor devices is Al, since it has a low electrical resistance compared to other materials and since it adheres well to insulating materials such as silicon oxide film. However, high-temperature treatment can cause silicon in the substrate to flow into the Al film and damage the junction in the area of the contact. This is referred to as an alloy spike. It lowers the breakdown voltage and causes shorts, especially in shallow junctions.

Countermeasures include adding silicon to the Al, and forming barrier metal between the Al and the silicon.

3.1.3 Increasing Gate Oxide Reliability with Hydrogen-Annealed Interstitial Wafers

When high temperature heat treatment is applied to silicon wafers in a hydrogen atmosphere, interstitial oxygen on the surface layer diffuses in an outward direction resulting in significantly fewer surface crystal defects (such defects are, in effect, oxygen deposits).

Figure 3.3 (a) shows the evaluation results for a defect-free surface layer formed on a hydrogen-annealed interstitial (HAI) wafer formed by annealing a CZ wafer with hydrogen at 1200 °C for one hour. The oxygen deposits on the surface layer (technically known as bulk micro-defects or BMDs) have been greatly reduced.

Advances in the fine-pattern processing of semiconductor devices have led to a reduction in gate oxide film thickness. The role that oxide film plays in the reliability of semiconductor devices calls for increased reliability of the gate oxide film. With much fewer surface crystal defects on the HAI wafer, as shown in the diagram, the percentage of defects in mode B of the oxide film breakdown voltage can be reduced (to zero). (See Figure 3.3 (b).)

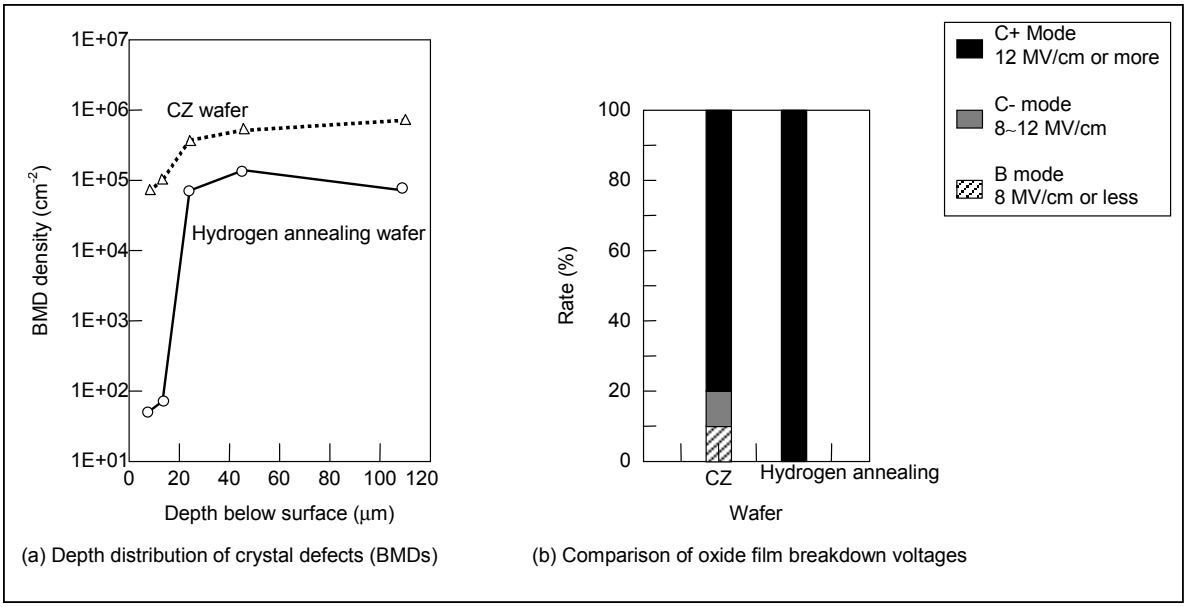


Figure 3.3 Effects of hydrogen-annealed wafer

3.2 Si-SiO_2 Interface

Semiconductor chips based on the surface phenomenon exhibit certain characteristics which vary significantly depending on the state of the Si-SiO_2 interface. There are many complicated failure mechanisms attributed to this phenomenon.

Failure mechanisms related to the Si-SiO_2 interface can be classified into those induced by the substrate and those induced by the gate oxide film or surface protective film. The former are described below. The latter are described in Section 3.3, Gate Oxide Film and Section 3.4, Passivation.

3.2.1 Degradation Due to Hot Carriers[2)]

When voltage is applied to the drain of an N-channel MOS transistor, a large electrical field is generated in the drain region as shown in Figure 3.4. As carriers flow into this area, they gain energy from the electrical field and become hot carriers. Some of them are scattered by phonons and others lose energy through impact ionization. Hot carriers with high enough energy to surmount the Si-SiO_2 energy barrier are injected into the gate oxide film. This phenomenon, which accelerates with increased voltage, changes the MOS transistor threshold voltage (V_{th}) and the transconductance (Gm).

Depending on the bias condition of MOS transistor, the carriers injected into and trapped within the gate oxide film are referred to as channel hot electrons, drain avalanche hot carriers (DAHC), secondary hot electrons or substrate hot electrons.[3)]

To avoid the effects of hot carriers, countermeasures are taken, such as reducing the circuit's internal operating voltage or creating a gate oxide film which does not easily trap injected hot carriers. Various measures are recommended for the transistor structure, especially for devices with a gate length of less than 2 μm. One of these is the lightly doped drain (LDD) transistor, shown in Figure 3.5, which exhibits a smaller electrical field around the drain and thus has fewer hot carriers.[4)]

Degradation of device characteristics due to hot carriers also occurs in bipolar transistors. This is a well-known phenomenon characterized by a reduced h_{FE} when a reverse bias is applied across the emitter-base. With the appearance of advanced shallow junction devices in recent years, there is a tendency towards increased reverse leakage current between the emitter and base and therefore a tendency towards greater degradation of characteristics due to hot carriers. Figure 3.6 shows an example of a degraded high-frequency characteristic (f_t) caused by reverse emitter-base bias. This is because the base current increases due to an increased number of recombination centers at the Si-SiO_2 interface caused by hot-carrier injection during reverse biasing.

Most semiconductor failure modes exhibit higher degradation rates at higher temperatures. The hot-carrier effect, however, accelerates as the temperature decreases.

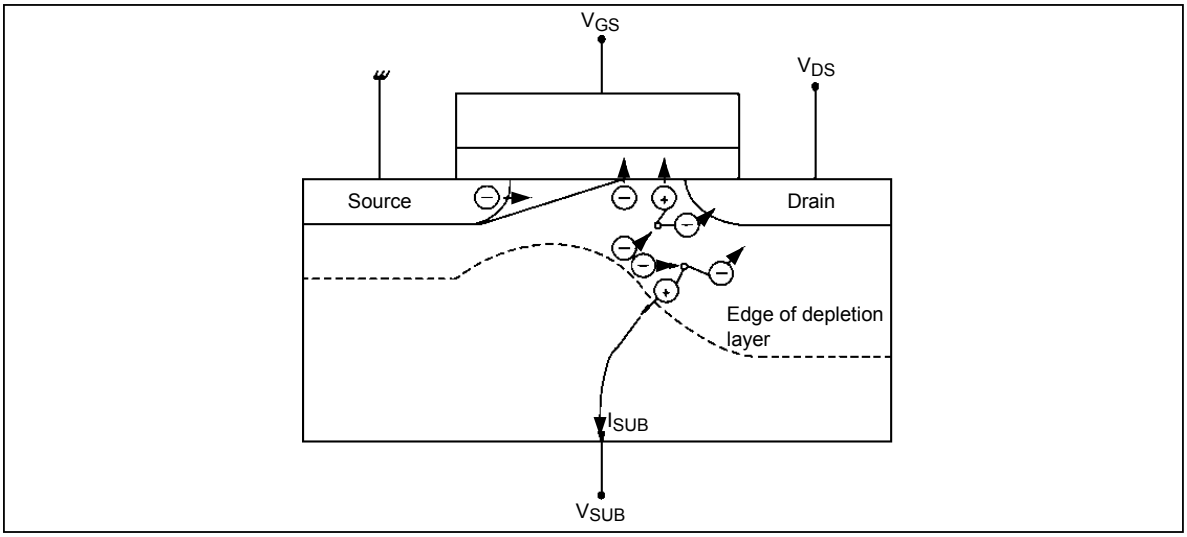


Figure 3.4 Hot-carrier injection model

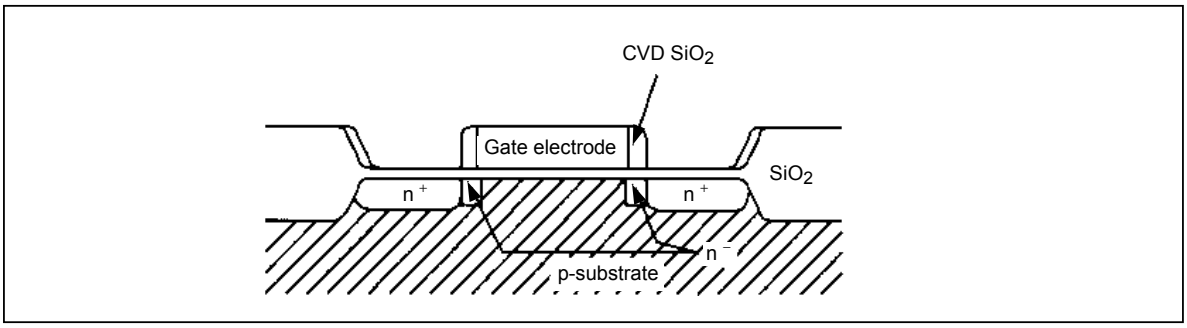


Figure 3.5 Lightly doped drain (LDD) structure transistor

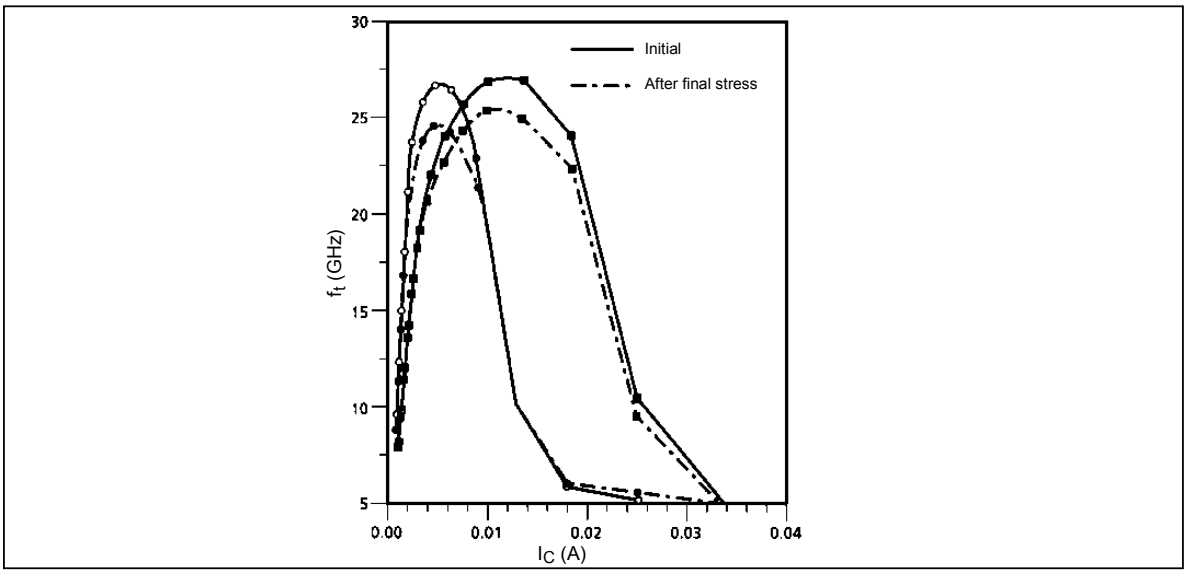


Figure 3.6 Degradation of high-frequency characteristics (f_t) due to reverse emitter-base bias

3.2.2 Noise Charge due to Impact Ionization[5)]

In the other failure mechanism caused by impact ionization, holes (in an N-channel device) from the electron-hole pairs generated by previous impact ionization are accelerated towards the substrate, causing secondary impact ionization. These pairs reach the immediately adjacent memory cells (CCD cells), filling storage capacitors with electrons and inverting their memory states. This failure mechanism should not be neglected, as scaling levels will become even greater in the future.

3.2.3 Soft Errors[6)]

With increasing device densities, errors caused by α-particle radiation from minute amounts of radioactive elements must be considered. These elements, such as uranium and thorium, are often contained in packaging and metal materials. Called "soft errors," device malfunctions due to radiation can broadly be classified into memory cell mode errors and bit line mode errors.

A memory cell mode error occurs when an α particle impinges on a DRAM cell capacitor (which is used to store one bit of information). Electrons generated by the impinging α particle and the resultant energy attenuation subsequently flow into the cell capacitor. In this mode therefore, a 1 in a cell capacitor is inverted to 0.

In a bit line mode error, electrons generated by α-particle radiation can affect the bit line information voltage or the reference voltage. In the former case 1s are inverted to 0s; in the latter case 0s are inverted to 1s. With increased cycle times, the probability of encountering a bit line signal error increases. Bit line mode errors, therefore, are dependent on cycle time while memory cell mode errors are not.

In order to reduce the soft error rate, measures such as applying high-purity resin and coating the chips to protect circuits from α-particle radiation are taken. Trench cell capacitors are used to increase the memory cell capacitance (see Figure 3.7).

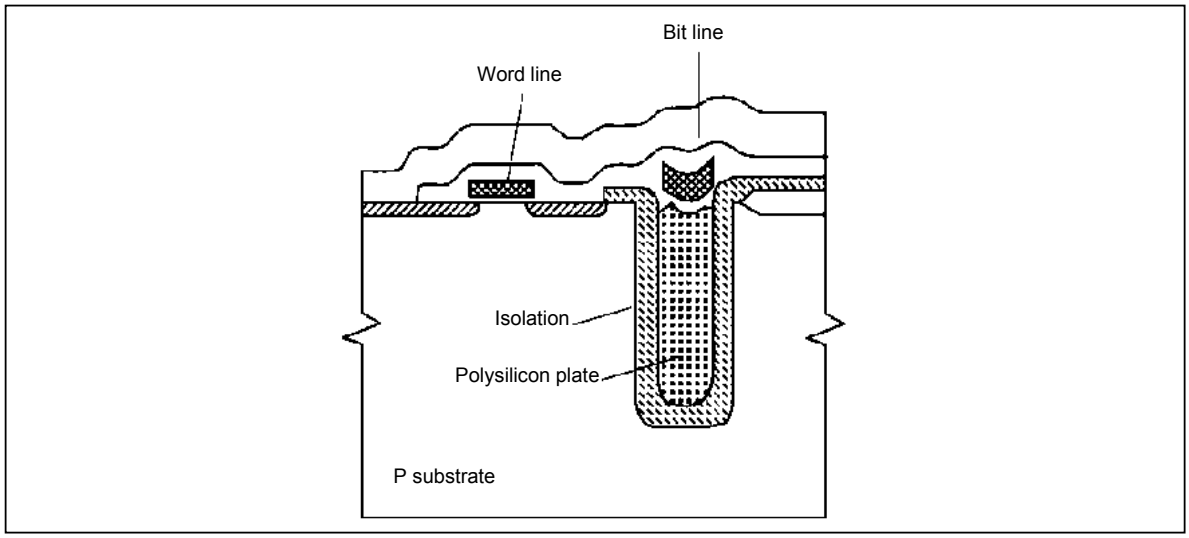


Figure 3.7 Example of trench cell structure

3.3 Gate Oxide Film

3.3.1 Oxide Film Breakdown

Since the gate oxide film of a MOS device is very thin (typically several nm~100 nm), applying a high voltage results in breakdown. For example, ESD or EOS can easily damage devices. During operation, the oxide film can be degraded over time. This is referred to as time dependent dielectric breakdown or TDDB.[7] Oxide film breakdown depends largely on the distribution of the oxide breakdown voltage, which is dependent on the intrinsic defect density in the gate oxide film. The oxide breakdown voltage and intrinsic defect density are affected in a complicated manner by many factors, including the gate electrode material, film thickness, defects in the substrate, oxidation method and contamination. They are also affected by the three-dimensional structure of the gate area, which is dependent on the design and fabrication process. The oxide breakdown voltage can only be improved to a limited extent by optimizing the fabrication process. Hence, protective circuits are added to prevent ESD or EOS.

In the case of TDDB, adding protective circuits is not effective because the breakdown of the oxide film occurs over a period of time, even if the device is operated below the typical oxide breakdown voltage. Degradation is greatly accelerated by an increase in the electric field, as expressed by the following equation:

$$Av = \exp(-\beta \cdot \Delta V)$$

β is the acceleration coefficient and depends on the oxide film thickness (T_{ox}) and fabrication process. The product of β and T_{ox} is nearly constant. Figure 3.8 shows the result of a voltage acceleration test performed by Toshiba.
In this case, $d = \beta \times T_{ox} = 41$ nm.

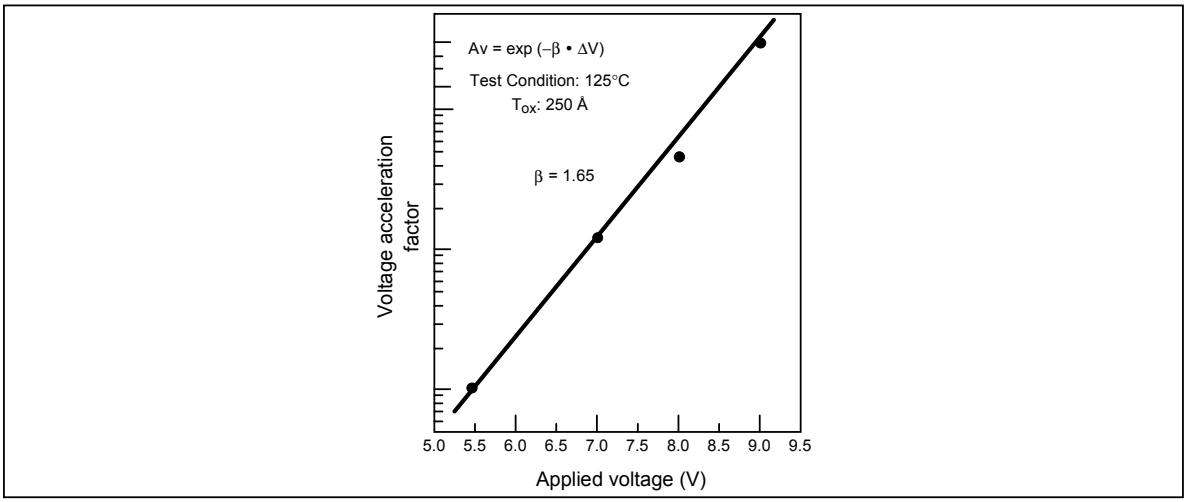


Figure 3.8 TDDB voltage acceleration

The temperature dependence of TDDB is not thought to be large and its failure distribution is known to be logarithmic. It has also been found that the TDDB failure rate depends greatly on the process, exhibiting higher rates for processes with a more dispersed oxide breakdown voltage distribution. Such process dispersions are considered to be caused by lot-to-lot variations.

3.3.2 Electrical Charges in Oxide Film

Certain instability phenomena are related to the electrical charges in the oxide film. The charges include ① mobile ions Q_m (Na^+, H^+), ② fixed charges Q_f, ③ oxide-trapped charges Q_{ot}, ④ the interfacial state Q_{it}, and ⑤ trapped charges generated by ionizing radiation. Figure 3.9 shows the charge states in the oxide film and interface. The instability due to mobile ions ① is believed to be caused primarily by contamination of the passivation film or by external contamination introduced into the process rather than the existing contamination of the gate oxide film itself. Charges ② and ③ do not change state due to surface potential. The degradation of threshold voltage occurs when these charges are generated within the oxide film. Charges generated near the interface between the gate oxide film and the Si substrate are referred to as fixed charges, and charges generated within the film are referred to as oxide film trapped charges. The interfacial state ④ changes in accordance with the surface potential and is referred to as "fast state." When this state occurs in the oxide film interface, the transconductance G_m is degraded. Charges ②, ③ and ④ are becoming important in new processes.

Furthermore, the advent in recent years of flash E^2PROM has given importance to the reliability of what is called the tunnel oxide film, a thin film of less than 10 nm through which electrons are exchanged. Repetitive write/erase operations in flash E^2PROMs cause trapped charges ③ in the oxide film, blocking the passage of electrons. It is also known that the trap state, or trapped charge, generates leakage in low electrical fields, causing loss of retained charge loss when the device is not in operation or during reads. Therefore, it is important to develop a tunnel oxide film with few traps to increase the number of rewrites and to improve charge-retention characteristics.

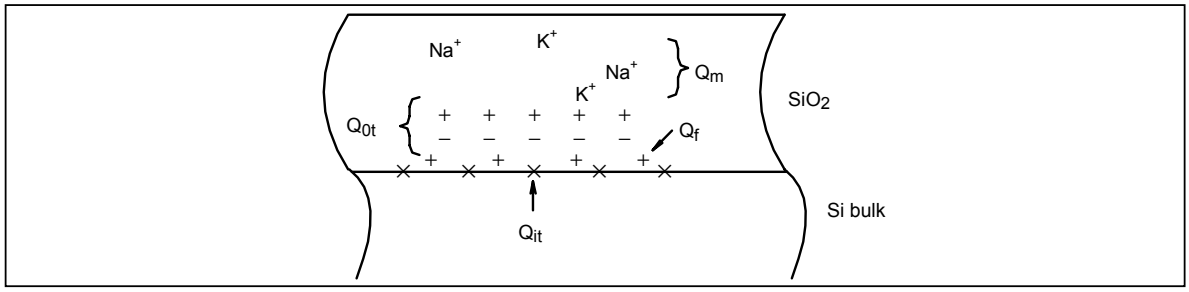


Figure 3.9 Charges in oxide film and interface[8)]

3.4 Passivation

Passivation has three primary objectives:

① Stabilization of the Si surface

② Creation of an interlayer insulating film in multilayered structures

③ Protection of the entire chip

Defects in passivation often lead to catastrophic failures. Such failures include unstable device operation caused by changes in film properties, instability, pin holes and cracks, and Al metal opens or corrosion due to degradation and stress. These factors are important when device reliability is considered. Symptoms of instability and degradation due to defective passivation include V_{th} shift and field leakage in MOS transistors, decreased h_{FE} in bipolar transistors, and breakdown voltage degradation in PN junctions.

These types of failure mode are known to be caused by the following mechanisms:

① Ion contamination

② Polarization

③ Parasitic MOS due to lateral extension of the electrical field

④ Corrosion of Al metal due to phosphorous in PSG, fluorine in plasma CVD oxide film or moisture penetration

⑤ Pin holes and cracks

⑥ Stress

⑦ Chip degradation due to degass[9)]

3.4.1 Ion Contamination

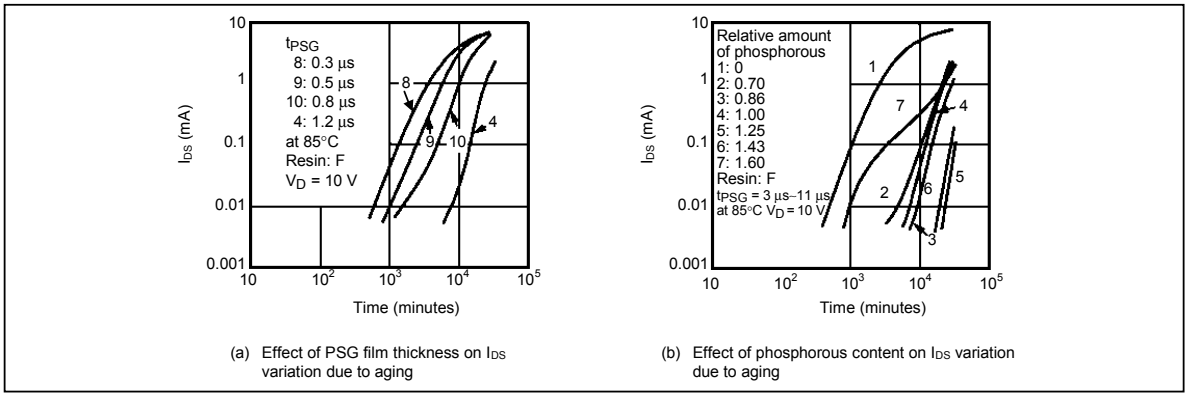
Contamination by Na^+ and other mobile ions introduced into the passivation or into the interface during the manufacturing process greatly affect device reliability.

The Na^+ ions are deactivated by phosphide gettering. However, application of an electrical field can cause them to move into the passivation oxide film and collect in the field region, gate region or around the PN junction, resulting in failures due to parasitic MOS, V_{th} change, breakdown voltage degradation etc. Breakdown voltage degradation can be recovered from by baking without bias. Like electrical field strength and temperature, humidity also accelerates degradation due to ion contamination.

Figure 3.10 shows experimental results for the external ion-blocking capability of phosphosilicate glass (PSG) with various film thicknesses and phosphorous contents.[10)] In the experiment, the test element group (TEG) device structure shown in Figure 3.11 was used on the assumption that ionic impurities from the mold resin pass through the PSG film and are accumulated on the gate oxide film which has no gate electrodes. This phenomenon causes a channel leakage current to flow between the drain and source whose level and variation with time are an indication of the ion-blocking effect of the passivation film. It can be understood from Figure 3.10 that the blocking effect increases with increased film thickness or phosphorous content. This rise in leakage current in the early stage can be

seen in the case of high phosphorous concentration. This is thought to be caused by ionic conduction accompanied by PSG moisture absorption.

The above-mentioned observations show why PSG is very often used for passivation. However, as evident from the experimental results, ionic degradation cannot be completely blocked, even using PSG. For this reason, silicon nitride film on PSG film, with its superior ion-blocking effect, is being used. Toshiba has also developed a nitride self-alignment (NSA) process to minimize ionic problems in bipolar ICs.



(a) Effect of PSG film thickness on I_{DS} variation due to aging

(b) Effect of phosphorous content on I_{DS} variation due to aging

Figure 3.10 Results of test of PSG ion-blocking effect

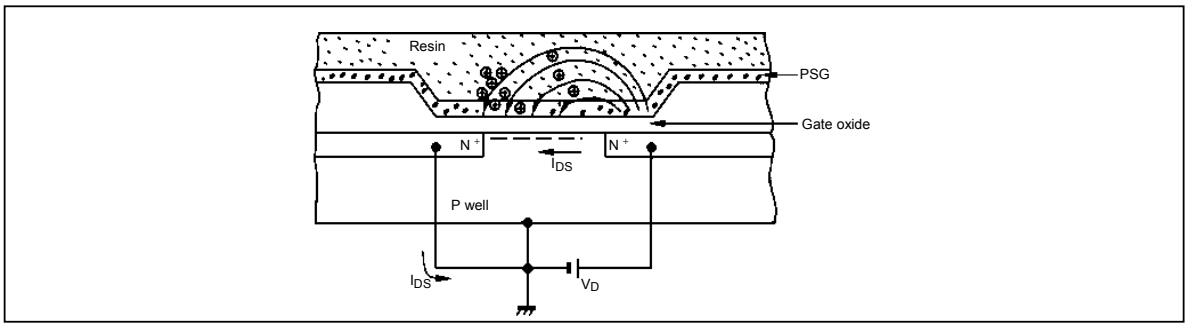


Figure 3.11 Structure of TEG device used in evaluation of PSG ion-blocking effect

Figure 3.12 compares the h_{FE} shift for the NSA process with the conventional process for bipolar transistors, using a high-temperature reverse bias test.[11] The NSA process exhibits no h_{FE} shift.

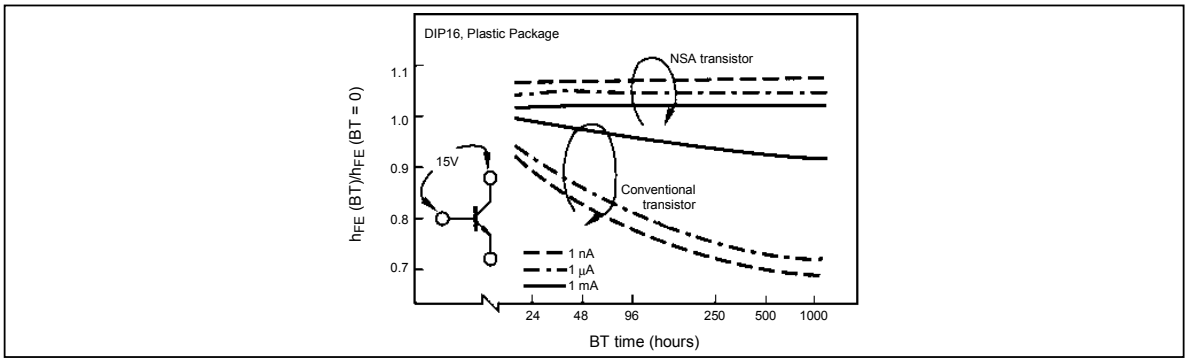


Figure 3.12 Change in current amplification factor (h_{FE}) during high-temperature reverse bias test

In the present submicron age, PSG has the drawback of not being able to fill narrow Al metal intervals. This has given rise to the use of plasma CVD oxide film due to its better coverage beneath the silicon nitride film.

3.4.2 Polarization

PSG provides ion-gettering and blocking effects as previously mentioned. On the other hand, increased phosphorous content causes polarization, resulting in various types of instability and degradation. [12)]

3.4.3 Parasitic MOS

As shown in Figure 3.13, if the surface SiO_2 becomes conductive, the electrode potential extends in a lateral direction to the adjacent PN junction forming parasitic MOS due to the inversion of the field region. Although measures against this type of failure mechanism are implemented during pattern and process design, there is still a small chance that the problem will occur, according to the humidity and ionic contamination in the external operating environment.

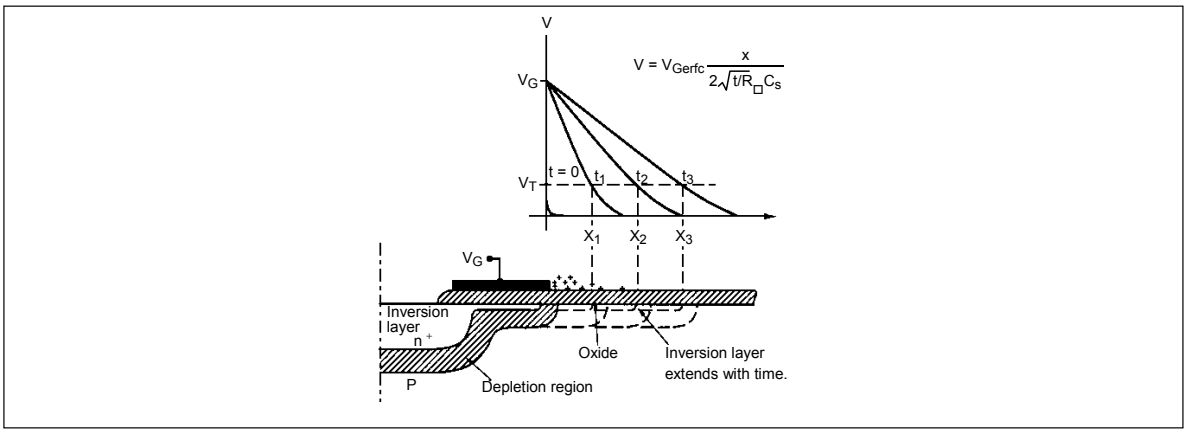


Figure 3.13 Model depicting extended charge in lateral direction[13)]

3.4.4 Al Metal Corrosion

Al metal corrosion caused by phosphorous in PSG is discussed in detail in the third paragraph of Section 3.5.3.

3.4.5 Pin holes and Cracks

If passivation includes a defect such as a pin hole or crack, interlayer shorting can occur in multilayered metallization. Also moisture, Na+ ions and other contaminants can enter, causing instability or degradation in the chip as well as Al corrosion. Cracks can be formed by thermal stress in the wafer process or due to mold distortion during assembly. The effects of mold distortion cannot be ignored, particularly with the increasing level of scaling in integrated circuit fabrication.

3.4.6 Stress

It is widely known that passivation stress affects the reliability of Al metallization. This is discussed in detail in Section 3.5.5.

3.5 Metallization

There are two kinds of metallization failure: the type that occurs where the metal contacts the silicon, and failure of the metal interconnections.

3.5.1 Contact Failure

It is well known that the scaling rule is applied to achieve high density. The diffusion junction depth underneath metal-to-diffusion contacts also becomes shallow in LSI and VLSI chips. However, Al metal and Si react during high-temperature processing to form alloy spikes. Contact between the metal and silicon fails when the underlying PN junction is shorted by the alloy spike. This failure mode is also caused by local heating by ESD stress and EOS. To avoid this problem, measures such as adding Si into the Al to suppress Al-Si reaction are generally used. Furthermore, barrier metal under the Al is used in submicron devices to prevent Al diffusion to the silicon.

3.5.2 Through-Hole Contact (Al-to-Al in a multilayered structure)

The scaling rule is also applied to through-hole contacts.

Therefore, open failures caused by Al step coverage at the step can occur. Also, when the through-hole open failures reach submicron levels, the difficulty of forming Al contacts necessitates the use of a via-plugs process.

3.5.3 Al Corrosion

Al corrosion is a major problem for reliability in plastic-encapsulated devices. Some instances have also been reported for hermetically sealed devices as well[14].
Following is a brief description of the Al corrosion mechanism in plastic-encapsulated devices.

(1) General model of Al corrosion
Figure 3.14 is a diagram of a plastic-encapsulated device. In general, plastic materials have moisture permeability and absorption properties. Epoxy resin and other materials have many kinds of cation and anion impurities that can inadvertently be introduced during assembly or other processing. When moisture is absorbed, ionic contaminants penetrate the chip surface. Cations or anions (depending on the applied bias) reach the Al surface by passing through micro-defects in the top passivation film, with the result that Al electrochemical reactions can occur. The result is a catastrophic failure such as an increase in Al interconnection resistance or an open.

This is the general mechanism of Al corrosion failure.

(2) Moisture penetration
The primary cause of Al corrosion is the intrusion of external moisture into the plastic package. Moisture is defined as water vapor in the atmosphere. There are two moisture penetration routes as shown in Figure 3.14. One is through the interface of the lead frame and the resin. The other is through the bulk and is dependent on the moisture permeability and absorption properties of the resin. It is difficult to determine which of these penetration routes is more likely to cause a higher rate of moisture penetration because they depend on factors such as operating environment and package type. Experimental data obtained through investigations using a moisture-sensitive chip encapsulated in a plastic package indicates that moisture penetration through the plastic bulk can be approximated by a diffusion model.[15]

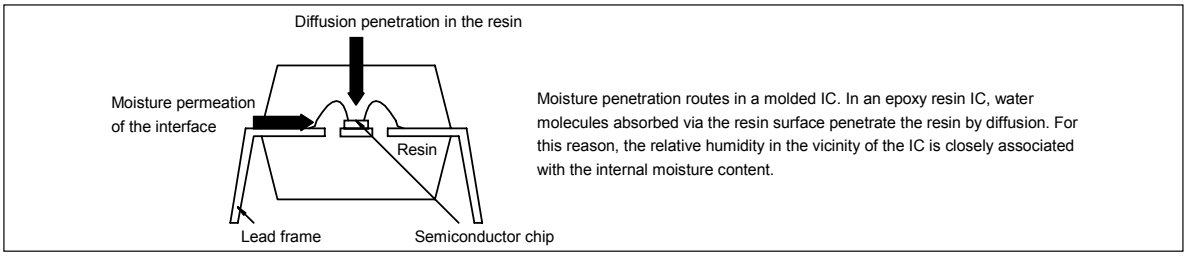


Figure 3.14 Plastic-encapsulated device

(3) Dependence on applied bias

As a result of temperature and humidity tests (80°C, 90% RH for the PSG passivation TEG with bias varied at 5 V, 10 V, 15 V, 20 V and 25 V), dependence of MTF on applied voltage was obtained as shown in Figure 3.15. It is apparent that the MTF decreases with increased bias voltage.

Al corrosion due to electrochemical reaction has different modes depending on the bias polarity. That is, the failure mechanism varies with the polarity. The biased terminal with the higher potential is called the "anode" and the terminal with the lower potential is called the "cathode." Al corrosion occurring on the anode and cathode sides is referred to as "anodic corrosion" and "cathodic corrosion" respectively. Cathodic corrosion is predominant in PSG passivation with Al and Al-Si metals; however, cracks or pinholes in the passivation can cause anodic corrosion due to impurity ions (for example Cl^-).

Cathodic corrosion occurs, in general, in the crystal grain boundary and appears dark when observed through an optical microscope. On the other hand, anodic corrosion is accompanied by a significant expansion of Al, sometimes causing cracks in the passivation which can propagate. In some instances, it appears as if the Al is missing when the device is observed under an optical microscope; however, it sometimes remains as transparent Al_2O_3, and can be identified using techniques such as electron probe microanalysis (EPMA) or Auger electron spectroscopy (AES).

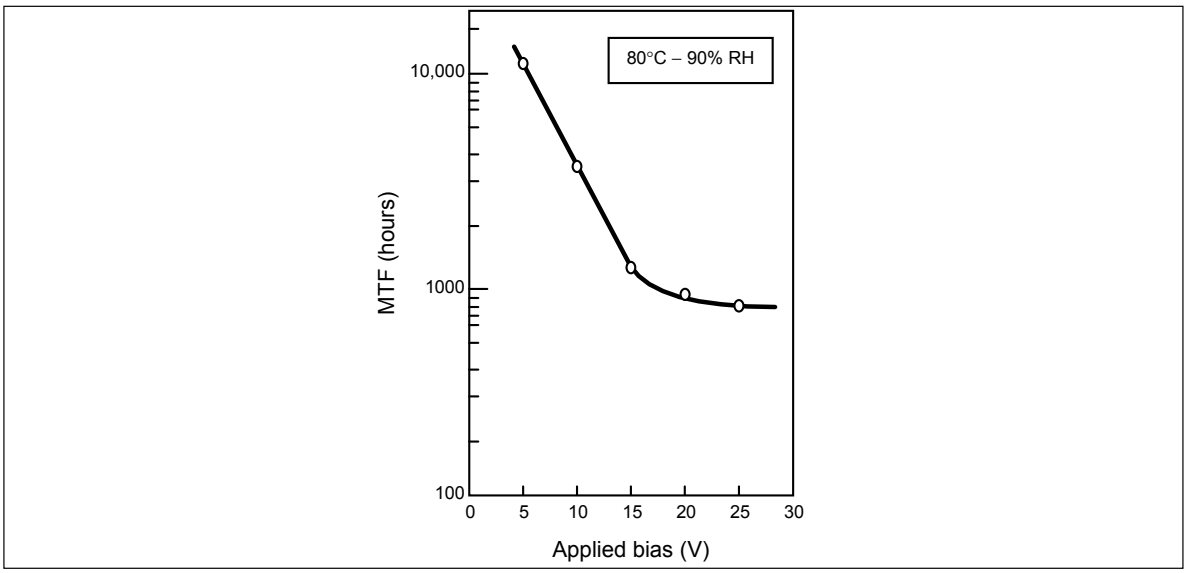


Figure 3.15 Dependence of MTF on bias voltage in THB test

(4) Dependence of PSG passivation on phosphorous concentration

It was previously described how, in order to subject the external ions to the gettering effect, PSG film containing phosphorous is used for top passivation. However, an excessively high concentration of phosphorous will greatly increase the possibility of fatal Al corrosion. Phosphorous-related corrosion is cathodic for Al or Al-Si metal and occurs as follows: [16) 17)]

First, if the PSG absorbs moisture, P_2O_5 in the PSG is liquefied to form phosphoric acid, increasing the ionic concentration. H^+ ions are attracted to the surface of the Al metal on the cathode side, allowing corrosion to progress according to the following reactions:

$Al + 3H^+ \rightarrow Al^{3+} + 3/2H_2\uparrow$
$Al^3 + 3OH^- \rightarrow Al(OH)_3$
and
$Al(OH)_3 + OH^- \rightarrow AlO_2 + 2H_2O$

Figure 3.16 shows relative lifetime values for TEG devices and LSIs versus phosphorous concentration in PSG, which causes cathodic corrosion. It shows that lifetime shift is very responsive to changes in phosphorous concentration. Recently, however, this type of failure has virtually been eliminated because moisture resistance has been improved by using films into which water cannot permeate (e.g. SiN films) for top passivation.

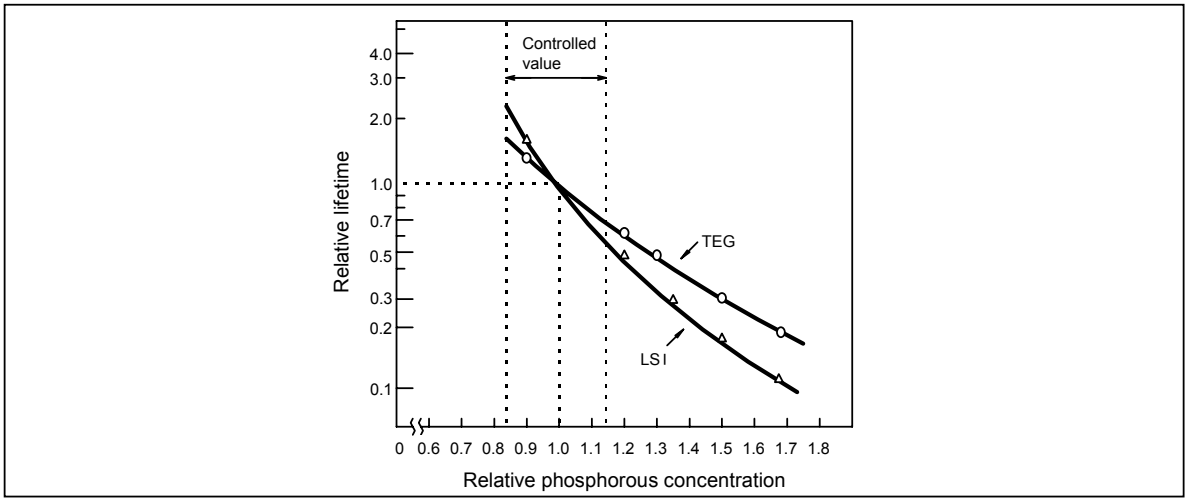


Figure 3.16 Dependence of relative lifetime on phosphorous concentration due to its influence on Al metal corrosion (experimentally controlled)

(5) Other unexpected events

In addition to the above items, factors contributing to Al corrosion include some that are attributable to the manufacturing process, such as defects and ionic contamination of top passivation, seal leaks in hermetically sealed devices, and improper handling or soldering by customers. Soldering flux, which contains Cl and water, can penetrate the plastic and corrode metal areas of the chip.

3.5.4 Electromigration

It is well-known that applying a high current to the Al metal in an IC device can cause an open failure. This phenomenon is called electromigration and is becoming an important failure mechanism as the scaling of ICs gets larger.

The following describes the mechanism of electromigration in thin metal film. If a large current flows in a thin film, electron wind force is applied to the metal atoms. As a result, Al atoms diffuse in the direction of electron flow (from cathode to anode), forming a void on the cathode side, and a hillock or whisker on the anode side.

An open failure on thin metal film can occur when the atomic flux in the metal achieves a positive divergence. This divergence of atomic flux is caused by variations in temperature or current density, or by a triple point of Al grain boundaries, for example, variable Al grain size,[18] a temperature increase due to heat generation inside the device,[19] or metal in contact with other material.[20]

The electromigration lifetime of the thin metal film is generally expressed as the MTTF (mean time to failure) as follows: [21]

$$MTTF = AJ^{-n}\exp\left(\frac{Ea}{kT}\right)$$

where J is the current density, n is a constant relating to the current density, Ea is the activation energy, T is the absolute temperature, k is Boltzmann's constant and A is a constant relating to the material type, structure and size of the metal. From this expression it can be seen that the MTTF increases with a decrease in current density or temperature. Also, the lifetime distribution approximates to a logarithmic distribution with a low variance.

Figure 3.17 shows an example of how to obtain the activation energy. A value of 0.6 eV is obtained for both Al-Si and Al-Si-Cu. The lifetime of Al-Si-Cu metal is longer than that of Al-Si metal. The addition of Cu to Al suppresses grain boundary diffusion, the dominant diffusion mechanism in electromigration.

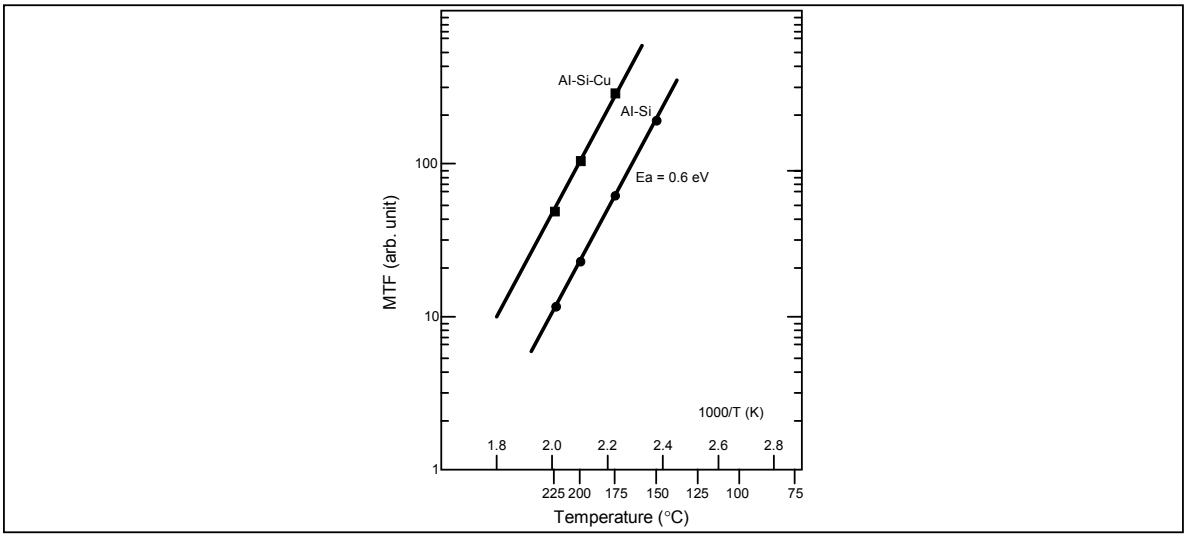


Figure 3.17 Temperature dependency of electromigration lifetime of metal

3.5.5 Stress Migration[22), 23), 24)]

When IC scaling reached the point where the width of the Al metal became less than 2 μm, Al open failures due to extended exposure to a high-temperature environment were reported.

This failure mechanism has been called stress migration and is considered to be caused by Al atoms migrating to relieve stress generated in the Al metal due to the difference between the thermal expansion coefficients of the Al metal and the passivation film of the interlayer insulator. It is known that this depends on the Al metal material, its deposition method and residual stress.[21)] Countermeasures, such as the addition of Cu to the Al metal, the use of barrier metal under the Al metal, and reducing passivation film stress, are taken to minimize this effect.

Acceleration of stress migration failure due to temperature does not occur uniformly because it depends on a combined mechanism of void diffusion and stress relief. However, it is known that the apparent activation energy at temperatures below 125°C is 0.7 eV for Al-Si and 0.9 eV for Al-Si-Cu.

3.6 Assembly

3.6.1 Chip Mounting

Chip mounting methods can be divided into ① Au-Si eutectic, ② solder, and ③ conductive paste, each having its own failure mechanisms. The solder and conductive paste methods are described below.

(1) Solder

Solder chip mounting is widely used for power transistors. However, in this case, thermal cyclic stress is generated through heating and natural cooling caused by repeatedly switching the transistor on and off, which accelerates the degradation of the solder bonding. This is referred to as thermal fatigue. Furthermore, the degradation of solder can increase thermal resistance, resulting in device breakdown due to local heat build-up.

Improving reliability where thermal fatigue is concerned is carried out primarily by proper selection of the soldering material and by controlling the environment of the solder bonding area. In the case of tin-antimony solder, the thermal fatigue characteristic varies significantly depending on the amount of antimony. Figure 3.18 shows the relationship between the amount of antimony and the failure rate, as determined in a thermal fatigue test. In the test, the device is repeatedly switched on and off 10,000 times until a junction temperature difference of 100°C is attained. Thermal resistance is then measured, showing the relationship between the amount of antimony and the failure rate (the device is assumed defective if its ΔV_{BE} reaches 1.2 × the initial value). The proper amount of antimony is found to be 8.0~10.5% by weight.[25)]

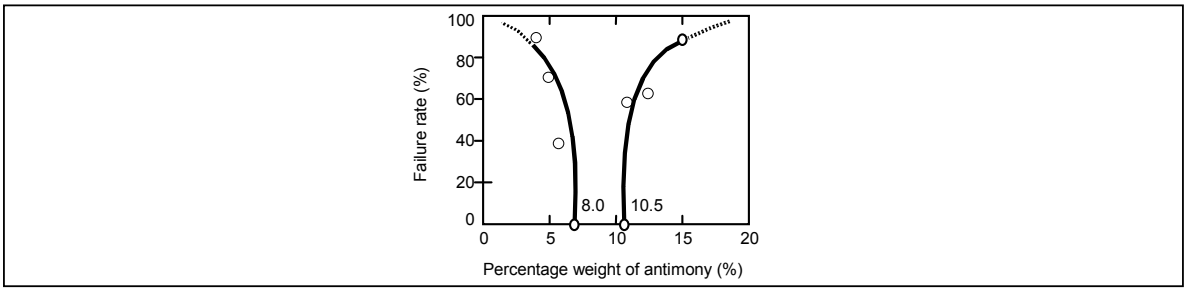


Figure 3.18 Antimony content versus thermal fatigue failure[25)]

(2) Conductive Paste

This method uses plastic resin adhesive to bond the die and the substrate. The adhesive consists mainly of epoxy or polyimide, usually prepared by mixing silver into the resin to provide electrical and thermal conductivity.

A problem with epoxy or polyimide adhesive is out-gassing generated by the materials, which can cause a failure due to corrosion, migration, surface leaks or V_{th} shift. Most of the out-gassing is moisture, with some components of amine or halogenide.[26)] Accordingly, careful consideration should be given to the adhesive agent used.

3.6.2 Wire Bonding

Wire bonding is the process whereby bonding pads on the die are connected to the leads. There are two methods: thermal compression and ultrasonic.

The wire bonding process, and the failure mechanisms which can occur during the process, are described below.

(1) Au-Al Intermetallic Formation

When bonding Au wire to Al, whereby the bonding surface is subjected to high temperature, a formation of purple alloy ($AuAl_2$), referred to as the "purple plague," is often observed. In contrast, when the proportion of Au is high, the Au_2Al alloy formed is referred to as the "white plague." The latter has higher electrical resistance and is mechanically weaker.

Since Au and Al have different diffusion constants, voids that degrade the bonding strength are formed at the intermetallic region, and resistance is increased. Bonding degradation will lead to open bond wires when mechanical or thermal stress is applied. However, such degradation can be considered negligible if the heating process is properly controlled during the manufacturing process.

(2) Mechanical Stress

With plastic-encapsulated devices, temperature cycling can cause excessive mechanical stress on bond wires due to the difference between the thermal expansion coefficients of the plastic resin and the bond wire. In some instances, this can result in an open bond wire. Also, wire deformation during molding can cause a situation in which a relatively high temperature will cause wires to come into contact with each other or with the edge of the chip, resulting in an electrical short. To prevent such problems, specific measures are taken involving optimization and/or automation of the assembly process, such as exerting control over the wire loop shape.

In hermetically sealed devices, bonding wires can open due to shock or vibration. This should be taken into account, particularly when ultrasonic cleaning is to be performed.

Furthermore, mechanical damage during bonding can, in some instances, cause secondary device failure. However, this problem can also be counteracted by optimization and/or automation of the manufacturing process.

3.7 Packages

3.7.1 Hermetic

(1) Airtightness

In the case of hermetically sealed devices, inadequate seals can cause moisture to penetrate into the chip cavity, causing device instability or Al corrosion. Similar problems will occur when moisture is introduced during the sealing process. During hermetic sealing, water vapor pressure in the sealing gas is strictly controlled using a dew point monitor. In MIL-STD-883D, Method 1018, the maximum allowable water vapor is specified, in terms of cubic volume ratio, as 5000 ppm at 100°C.

In the case of Cerdip packages it has been reported that water vapor can evolve from the glass component during sealing and become trapped within the cavity causing Al corrosion.[14)]

This problem will soon be resolved with improved sealing glass.

(2) Electrochemical Migration of External Leads

Since a ceramic package is not as hydrophobic as a plastic one, sudden temperature changes in the ambient environment can allow water vapor in the air to be adsorbed on the surface, causing electrochemical migration of plating metal between the leads, which can eventually cause a short. This mechanism is accelerated by ionic contamination of the lead surface and by applied voltage. Therefore, special care must be taken when handling the devices, as well as with the operating conditions. Resin coating has been found to be effective in preventing electrochemical migration between leads.

(3) α-Particle Irradiation from Package Materials

With increased chip density in memory and CCD devices, bit error problems caused by α particles have become significant. The primary source of α particles, U and Th, are found in package material in relatively low amounts.[27)] To reduce the influence of α particles, chips are usually covered with a thick coating of polyimide, or circuits with a strong resistance to α particles are used.

(4) Miscellaneous Problems

In the case of ceramic packages, seal leaks and Al corrosion can be caused by cracks resulting from an excessive mechanical shock.

In the case of hermetically sealed devices, metal scattering inside the cavity can occur during the sealing process. This loose foreign matter can cause shorts. A particle impact noise detector (PIND) test is used to detect internal foreign matter.

3.7.2 Plastic-Encapsulated

(1) Ionic Impurities in Plastic Resin

As described previously, with plastic-encapsulated devices, instability in and degradation of device characteristics or Al corrosion can occur due to ionic impurities in the resin material. Accordingly, encapsulation must be performed using resin that contains low levels of ionic impurities so as to improve moisture resistance. Ionic impurities in the resin are estimated using

the hot water extraction method. Of the various ionic impurities, the Cl^- ion in particular is considered to have a pronounced effect on moisture resistance.

The following are the results of an experiment conducted to determine the correlation between device instability and Al corrosion caused by ionic substances in the resin.[10)]

As already mentioned, formation of parasitic MOS due to the accumulation of ions is one of the typical mechanisms of device degradation caused by ionic impurities in the resin. Utilizing this phenomenon, it is possible to evaluate the ionic substance in the resin by the ion accumulation rates on the gate oxide film, as shown in Figure 3.19 (a). This is done by applying bias at high temperature to the drain of an ion-sensitive TEG device after it has been sealed.

The ion accumulation model can be represented by the equivalent circuit shown in Figure 3.19 (c). This model is based on the bulk resistivity ρv (which is proportional to the bulk resistance Rr). The bulk resistivity is the reciprocal of the bulk conductivity, which in turn is proportional to the concentration of ionic impurities in the resin multiplied by the ionic charge multiplied by the ion mobility. The model also includes the resin-SiO_2 interface resistance R and the oxide film's equivalent capacitance C_{ox}.

The potential of the oxide film surface (equivalent gate voltage V_G*) when
R >> Rr can be approximated by the expression:

$$V_G^* \approx V_A\left\{1-\exp\left(-\frac{t}{\tau}\right)\right\}$$

where V_A is the saturated value of V_G*, and τ equals C_{ox}* • Rr, a time constant dependent on the bulk resistance of the resin. Thus Rr, ρv and τ are interrelated. From this, it can be seen that the smaller ρv or Rr, the larger the ion conductivity and consequently, the greater the number of ions which reach the surface. This leads easily to unstable device characteristics and Al corrosion.

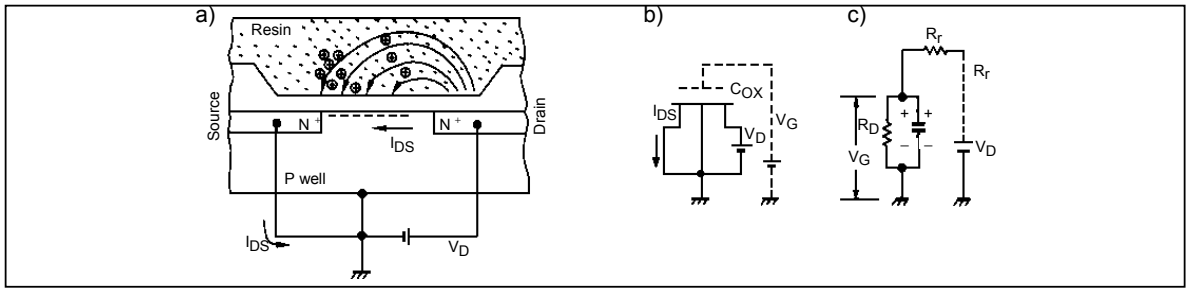


Figure 3.19 Charge accumulation model

Figure 3.20 correlates τ, described above, and the rate of Al corrosion. Al corrosion diminishes as τ becomes larger.

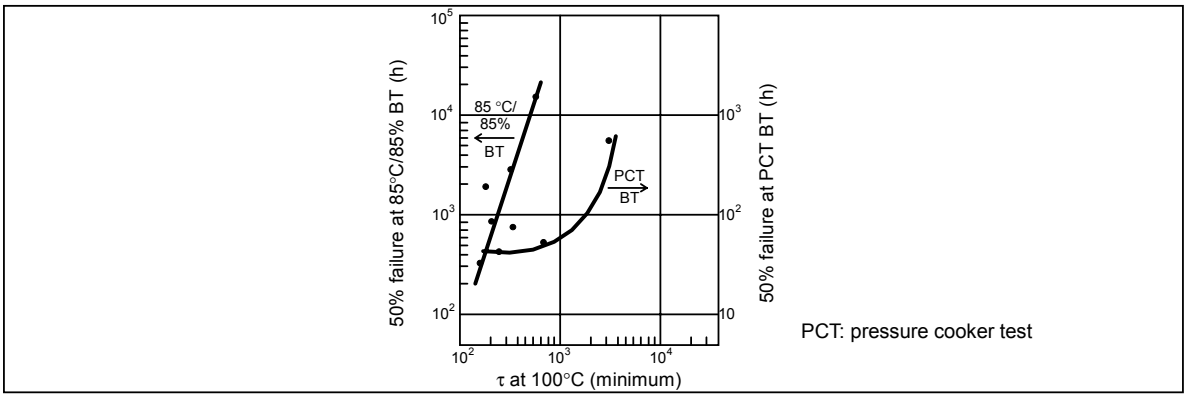


Figure 3.20 Correlation between time constant of channel leak and Al corrosion at high temperature

Figure 3.21 shows the temperature dependency of τ. The activation energy is estimated to be approximately 0.9 eV to 1.0 eV, which conforms to the temperature dependency of bulk resistance of resin shown in Figure 3.22. Figure 3.23 shows the degradation of bulk resistance due to moisture absorption. It clearly indicates that bulk resistance degrades as an exponential function of moisture absorption.

From the above, it can be said that high-temperature bulk resistance of resin and bulk resistance degradation by temperature and humidity are the important parameters in estimating resin reliability.

In addition, the adhesive property between the chip surface and metal, moisture permeability and moisture absorption are also factors with a bearing on the moisture resistance of the resin. In general, silicone resin features high moisture permeability, low moisture adsorption, good adhesion to the chip surface and poor adhesion to the metal. Epoxy resin has properties almost opposite to that of silicone resin. The drawbacks of epoxy resin are gradually disappearing as improvements continue to be made.

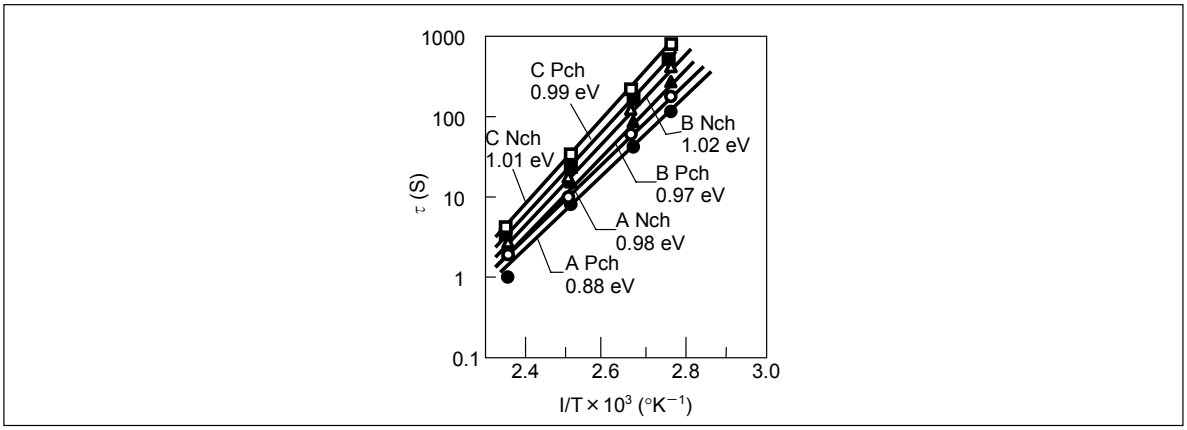


Figure 3.21 Temperature dependency of time constant τ

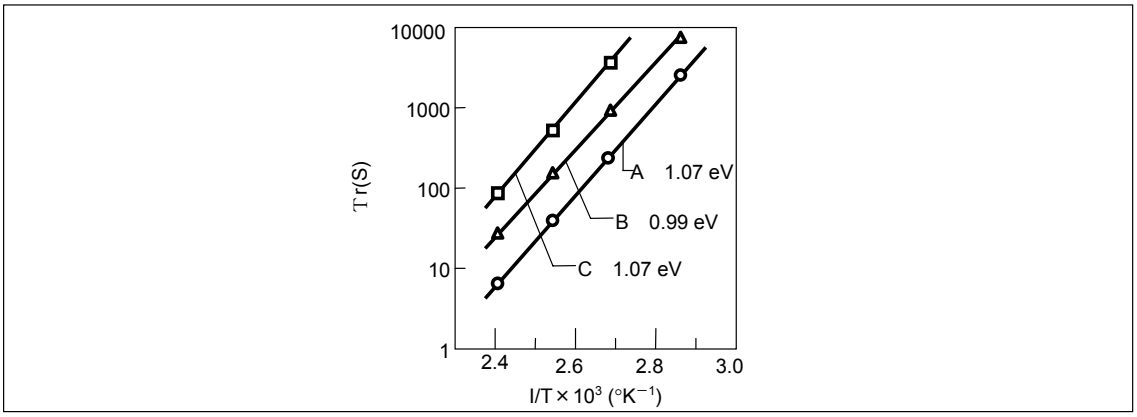


Figure 3.22 Temperature dependency of time constant (τ_R) for different discharge characteristics

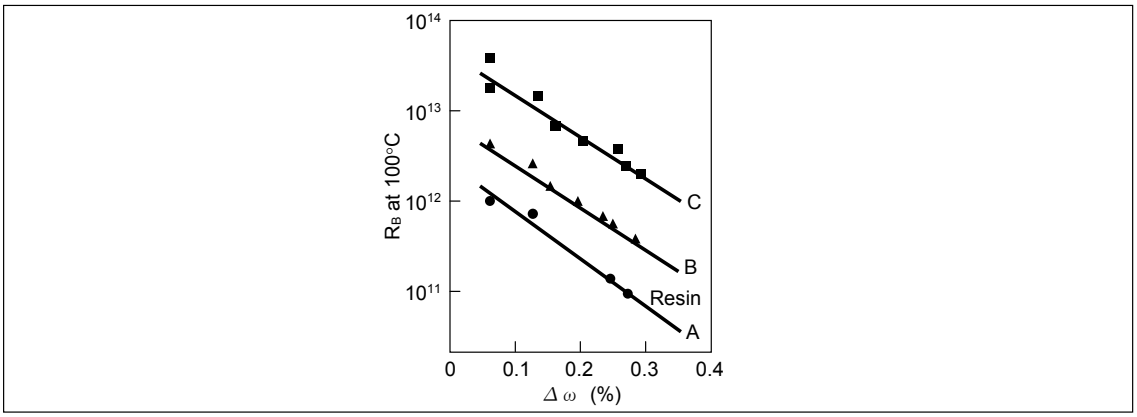


Figure 3.23 Absorbed moisture dependency of bulk resistance

(2) Various Problems Caused by Mold Resin Stress

Resin used for semiconductor encapsulation contracts due to resin polymerization, applying considerable stress to the semiconductor chip in contact with the resin. Consequently, resistor values in the chip fluctuate due to piezo-resistance, greatly affecting device characteristics. Stress also causes Al slide and passivation cracks. An experiment to determine the stress generated in a plastic-encapsulated silicon chip is discussed below.[23)]

Stress is measured on TEG devices which have resistors constructed on the silicon chip as shown in expression 3.1. A general formula for the piezo-resistance effect is:

$$\delta\rho i = \left(\frac{\Delta R}{R}\right) i = \sum_{i=1}^{6} \pi ij \cdot \tau j \quad \text{-------- } 3.1$$

where $\delta\rho_i$ is the resistance change rate, πij is the piezo-resistance coefficient and τj is the stress. For τj, the following applies:

$$\tau 1 = \sigma_x, \quad \tau 2 = \sigma_y, \quad \tau 3 = \sigma_z \quad \text{-------- } 3.2$$
$$\tau 4 = \sigma_{yz}, \quad \tau 5 = \sigma_{zx}, \quad \tau 6 = \sigma_{xy}$$

Since a silicon chip is quite thin, it can be assumed that σ_x; $\sigma_y >> \sigma_z$. In addition, the piezo-resistance coefficient πíj is the tensor of the fourth order determined by the semiconductor conductivity type, crystal orientation, direction of resistors and impurities that are present. The value of πíj can be determined by applying a given stress for which these parameters are known to the TEG devices. From expressions 2.3.1 and 2.3.2, the stress is determined as follows:

$$\sigma x = \frac{1}{2}+\left(\frac{1}{A}+\frac{1}{B}\right)\delta\rho 1+\frac{1}{2}\left(\frac{1}{A}-\frac{1}{B}\right)\delta\rho 3$$

$$\sigma y = \frac{1}{2}+\left(\frac{1}{A}-\frac{1}{B}\right)\delta\rho 1+\frac{1}{2}\left(\frac{1}{A}+\frac{1}{B}\right)\delta\rho 3$$

$$\sigma xy = \frac{1}{C}(\delta\rho 2-\delta\rho 4)$$

Where coefficients A, B and C are shown in Table 3.1.

Table 3.1 Coefficients used in stress measurement[23)]

Orientation \ Coefficient	A	B	C
100	$\pi_{11}+\pi_{12}$	$-\pi_{44}$	$-2(\pi_{11}-\pi_{12})$
111	$\pi'_{11}+\pi'_{12}$	$-\pi'_{11}+\pi'_{12}$	$-2(\pi'_{11}-\pi'_{12})$

Table 3.2 shows stress measurements when a TEG device with a chip size of 3 mm^2 is encapsulated in a 16-pin DIP. Stress is determined for the chip while it is in wafer form. Internal chip stress is found to be non-uniform, larger in a longitudinal direction at the center, and different at the center and periphery.

Table 3.2 Measured mean stress using {100} P-type resistors[29)]

Unit: N/cm^2

Location \ Process		Mount	Mold	Cure 2H
a Center	σx	-4312	-11760	-16072
	σy	-5292	-16366	-22050
	Zxy	107.8	-58.8	39.2
b Peripheral	σx	-4018	-6076	-11564
	σy	-5880	-7154	-13524
	Zxy	245	1479.8	1783.6

Figure 3.24 shows the TEG deivice used to determine the distribution of internal chip stress. Resistors arranged in the three directions shown in (b) are treated as a unit, with 55 units to a chip.

Figure 3.25 show the distribution of stresses σ_x, σ_y and π_{xy} after encapsulation. These experimental results are conveyed to the design department.[28)]

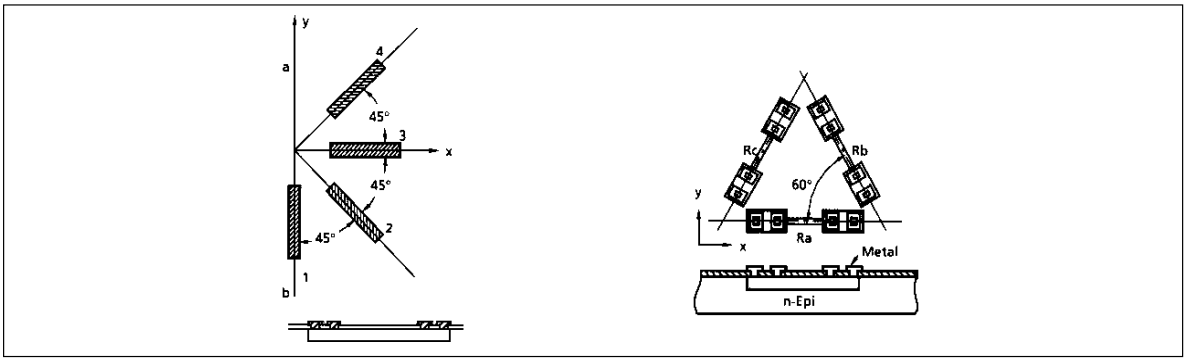


Figure 3.24 Structure of resistor TEG[28), 29)]

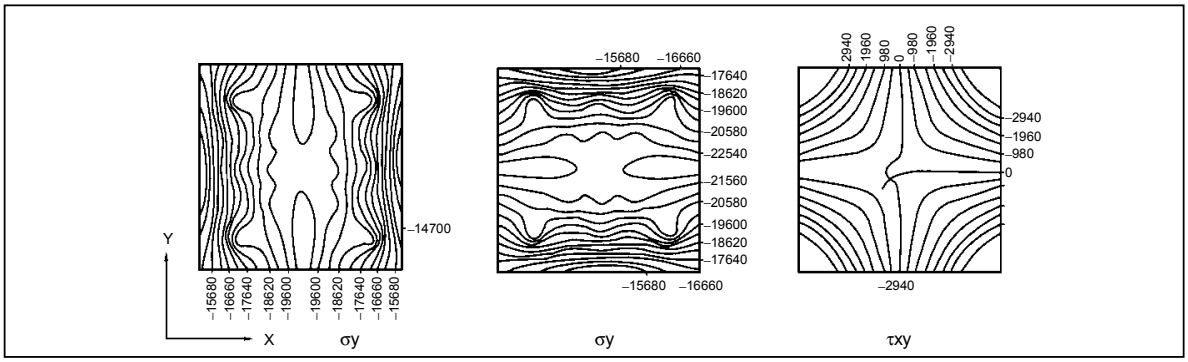


Figure 3.25 Stress distribution after encapsulation[28)]

(3) Top Passivation Crack Caused by Fillers in Mold Resin[30)]

Mold resins contain SiO_2 fillers. When these fillers exist in the interface between the die and the resin, cracks can be formed in the passivation due to the stress from TCT and other thermal factors. As a result, the Al beneath the crack deforms, and the crack can extend to the interlayer film beneath the Al. This can form a leakage path in the crack and cause a leak between the Al and the poly-Si beneath the Al, resulting in device failure. A countermeasure is to apply a polyimide coating to the die surface.

(4) Effect on Reliability of Soldering Stress in Surface-Mounted Devices

Plastic-encapsulated packages, which are easily molded, are fabricated in various shapes. Consequently, a wide variety of surface-mount products have been developed so as to increase the IC density on circuit boards.

Compared to board-insertion packages such as DIPs and SIPs, surface-mount devices are prone to package cracks and degradation of moisture resistance. This is because there is a greater chance for the mold resin to be exposed directly to heat during mounting. Recently, the trend towards using slim-profile packages and increased chip sizes make surfac-mount devices (SMDs) even more susceptible to thermal stress during soldering.

The reliability of surface-mount packages is, in most cases, determined primarily by the soldering conditions. Therefore, when devices are mounted on a circuit board, moisture absorption control and soldering conditions must be carefully considered.

The following is a discussion of the reliability of surface-mount packages in relation to moisture absorption and moisture removal characteristics, and package cracks due to soldering heat.

(a) Package Moisture Absorption and Moisture Removal

Resin used for plastic-encapsulated devices is basically porous and has some moisture permeability. In the case of SMDs, in areas where the mold resin is especially thin moisture can pose a significant reliability problem. This can occur during soldering when moisture, absorbed into the package, evaporates with a sudden rise in temperature, causing the package itself to expand or gaps to form between the lead frame and resin. There is therefore a close relationship between the amount of moisture absorbed by the SMD package and its reliability after soldering. The following discusses moisture absorption and moisture removal in an SMD.

- Moisture Absorption

  Figure 3.26 shows the moisture absorption characteristics of an 80-pin QFP in a shelf environment (with constant temperature and varying relative humidity). The horizontal axis indicates the time that the device remains on the shelf, and the vertical axis indicates the rate of change in the amount of moisture absorbed. The rate of change in moisture absorption is a percentage value given by dividing the amount of moisture absorbed by the weight of the package at the start of the shelf test. This diagram reveals that, when the temperature is low, more time is required for the saturation region to be reached; and when the relative humidity is low, the amount of moisture absorbed at saturation is smaller.

  Figure 3.27 shows comparative data for the moisture absorption characteristics of an 80-pin QFP (with a mold resin thickness of 2.7 mm) and a 20-pin SOP (with a mold resin thickness of 1.5 mm) in a shelf environment (at a temperature of 85°C and relative humidity of 85%RH). As evident from this diagram, the time to saturated moisture absorption varies with the package size. When real products are being tested for the effects of soldering heat, the products under test are forced to absorb moisture prior to testing, so that each package can be evaluated with different moisture absorption times.

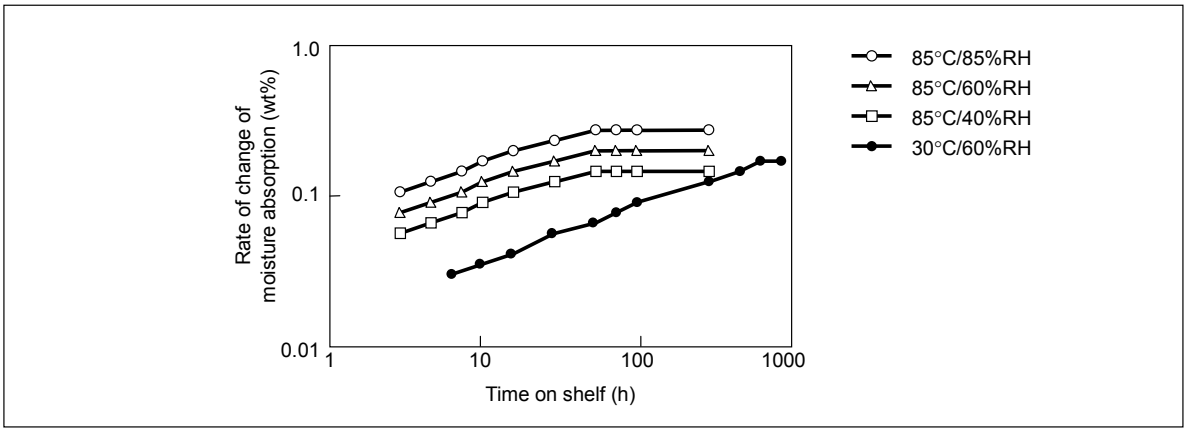


Figure 3.26 Moisture absorption characteristics of 80-pin QFPs (2.7 mm thick) in various environments

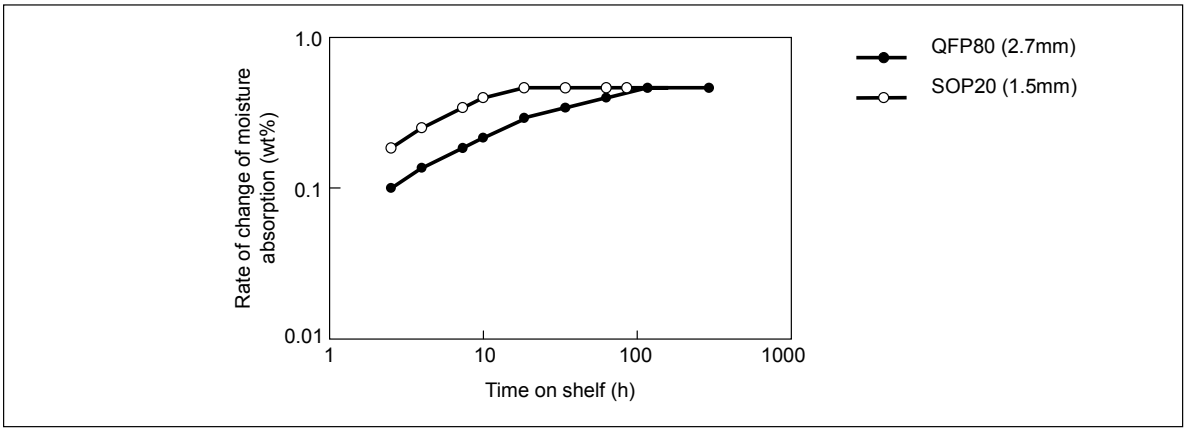


Figure 3.27 Comparison of moisture absorption characteristics of packages at 85°C, 85% RH

- Moisture Removal

  Devices with a large package or large chip size, or those housed in a thin package, are subject to limitations with respect to their soldering mount methods. This is because if the package contains moisture, soldering heat during mounting damages the package as described above. To prevent this problem, the device must be baked to remove internal moisture before it is soldered to the board.

  Figure 3.28 shows moisture removal characteristics for an 80-pin QFP (with mold resin thickness 2.7 mm) in a shelf environment. The horizontal axis is the time the device is left on the shelf, and the vertical axis is the rate of change of residual moisture content in the package, expressed as wt%. The diagram shows that even a package that has become saturated with absorbed moisture can have almost all moisture removed by baking at 125°C for 20 hours. Moisture removal characteristics are similar to those of moisture absorption in that the higher the temperature, the less time required for moisture removal, with residual moisture after baking approaching 0%. However, note that when removing moisture from devices, the baking temperature is subject to limitations depending on the thermal resistance of the tray and the device terminals' soldering properties. Before baking, refer to the instructions on the product packaging material or contact the manufacturer.

  Note that heat-resistant trays are marked "HEAT PROOF", meaning that they can normally resist temperatures of up to 125°C.

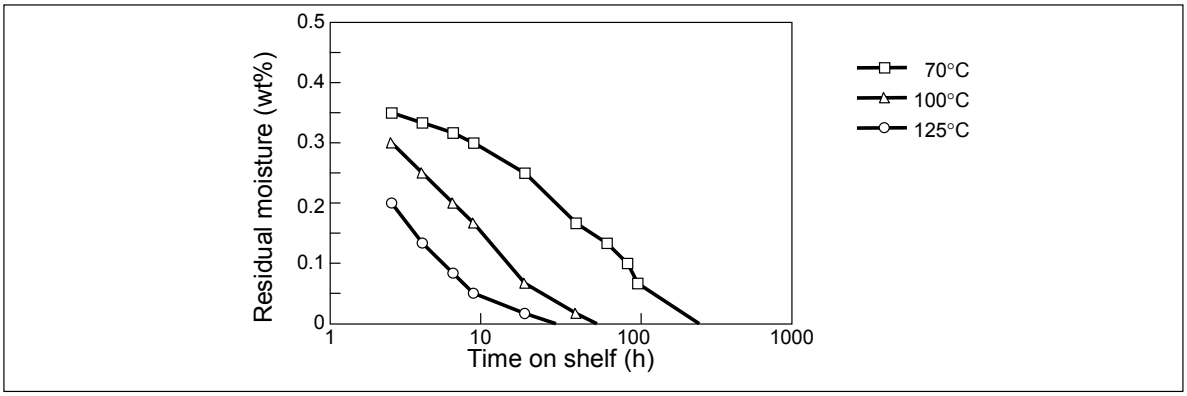


Figure 3.28 Moisture removal characteristics of 80-pin QFPs (2.7 mm thick) in various shelf environments

(b) Package cracking mechanism

Figure 3.29 shows the process by which package cracks occur. Such cracking is attributable mainly to expansion when moisture which has collected beneath the die pads evaporates.

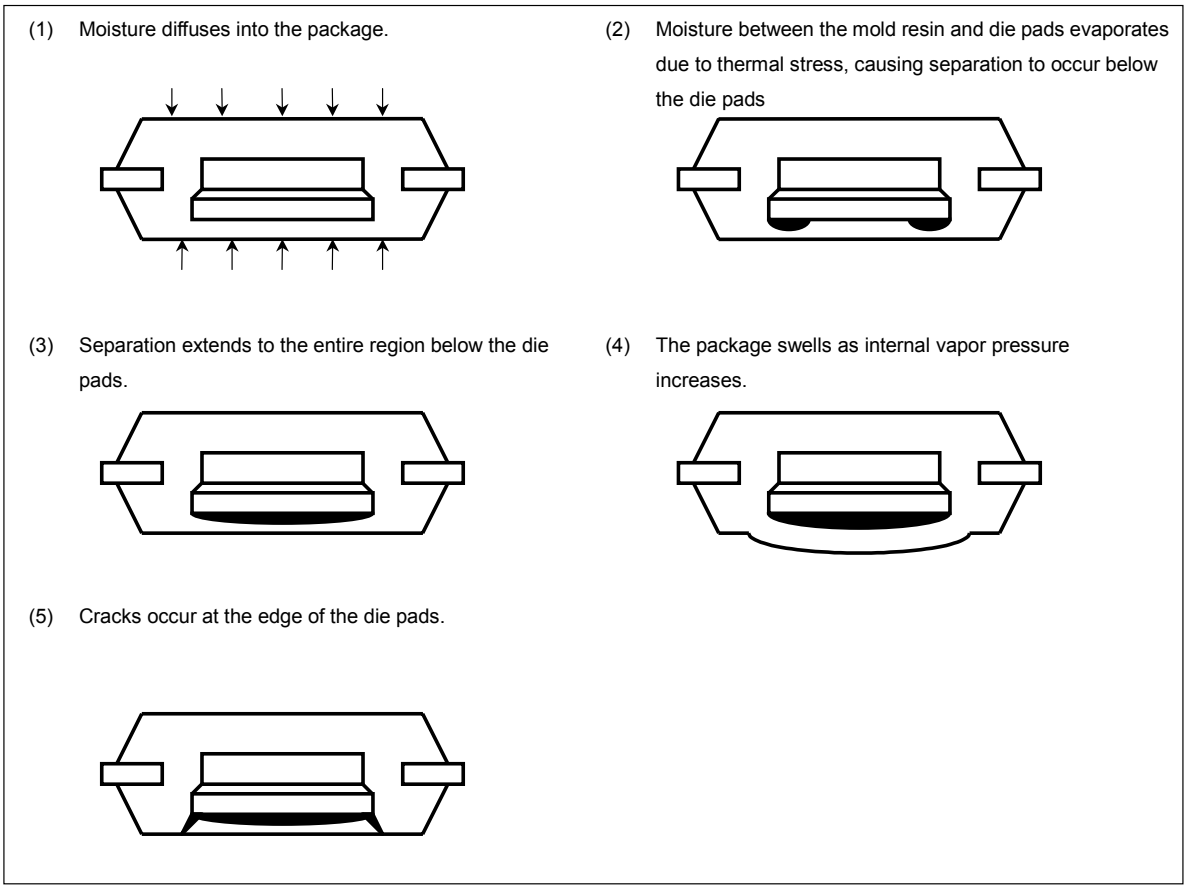


Figure 3.29 Package cracking mechanism

(5) Others

Since resin has a higher thermal resistance than metal, if thermal dissipation is inadequate, the chip temperature will increase, degrading operating margins or materials and causing the device to fail. To prevent this, countermeasures such as increasing the thermal conductivity of the resin or attaching heat sinks are taken.

However, various failures can still occur if the ambient temperature or power dissipation exceeds the absolute maximum rating.

Plastic-encapsulated devices can ignite at extremely high temperatures. This can occur with several of the failure mechanisms described above. Toshiba are now making Flame-resistant resins which conform to the current standard for resin non-flammability contained in the U.S. Underwriter's Lab Inc. (UL) Standard.

3.8 Electrostatic Discharge

3.8.1 Overview

As semiconductor devices undergo increasingly higher levels of fine-pattern processing and circuit integration, performance has improved at a phenomenal rate. However, as a result, these same devices have become increasingly susceptible to electrostatic discharge (ESD), making device degradation and damage from ESD a major problem.

This section describes how electrostatic discharge occurs and how it inflicts damage on devices.

(1) ESD Model

(a) Human Body Model (HBM)
In this model the human body serves as the source of static charge. Discharges of static electricity from the body can damage devices. Although there are various discussions concerning how much static charge the human body is capable of containing, evaluations are generally conducted using a 100-pF, 1500-Ω capacitor discharge arrangement.

(b) Machine Model (MM)
In this model objects with a high static charge capacity, such as device-handling equipment constructed of metal, serve as the source of static charge. A discharge of electricity from such an object under low-resistance conditions can damage devices. Evaluations are conducted using a 200-pF, 0-Ω capacitor discharge arrangement.

(c) Charged Device Model (CDM)
In this model the device itself becomes the source of static electricity due to friction. As the device approaches a charged body, a sudden discharge of electricity through the leads damages the device.
Evaluations are conducted using dedicated CDM test equipment.

(d) Others
In addition to the above ESD models, there is the field-induced model (FIM), in which induced electrification occurs when a device with an insulated structure, such as a MOS device, is exposed to a high-level electrical field source, discharge from which damages the device. There is also a small-size capacitor method (10-pF, 0-Ω) that approximates CDM using the capacitor discharge method.

(2) Breakdown Modes

(a) Oxide Film Breakdown
The dielectric breakdown strength of oxide film is generally reported to be 8 MV/cm~10 MV/cm. For this reason, devices with a thin oxide film, e.g. 50 nm, experience dielectric breakdown at 40 V~50 V. Since MOS devices can experience damage at low voltages, care must be taken to handle them in ESD-protected environments.
Oxide film breakdown in a MOS structure occurs when voltage above the tolerable level is applied to oxide film with low thermal conductivity, or when a level of energy sufficient to inflict damage is dissipated in the MOS device.

(b) Junction Breakdown
Junction breakdown occurs when excessive current flow raises the junction temperature

enough to destroy it with heat. The Wunsch & Bell model, with its thermal diffusion formula, is commonly used to describe this failure mechanism. [31] In the model, the junction breakdown phenomenon is determined from the pulse width and power density that are applied to the device.

Since junction energy consumption differs for a forward or a reverse discharge, different breakdown voltages result. Electrical discharge in a forward direction does not concentrate energy in localized areas as a reverse discharge does. Consequently the breakdown voltage for a forward discharge is higher than that for a reverse discharge.

(c) Metallization Breakdown

Metallization breakdown, like junction breakdown, is caused by thermal destruction. It is thought to occur when the power density (the amount of heat) reaches a level sufficient to fuse metal.

3.8.2 Latch-up

MOS and CMOS ICs are destroyed in some instances when an excessive voltage causes a parasitic thyristor to conduct.

Figure 3.30 shows a CMOS sectional structure. As shown, CMOS has NPN and PNP parasitic transistors which constitute the PNPN thyristor structure shown in Figure 3.30. If a voltage greater than V_{DD} max is applied to pin D, for example, the emitter-to-base of Tr1 becomes forward-biased. The collector current in Tr1 drops to GND through R_P causing a potential difference to develop across R_P. This in turn forward-biases the emitter-to-base of Tr2 so that the collector current in Tr2 is sourced from V_{DD} through R_N, causing a potential difference to develop across R_N. Consequently, greater and greater amounts of positive feedback are applied, forward-biasing the base-to-emitter in Tr1 and forcing the thyristor structure to conduct. Eventually, the CMOS device breaks down.

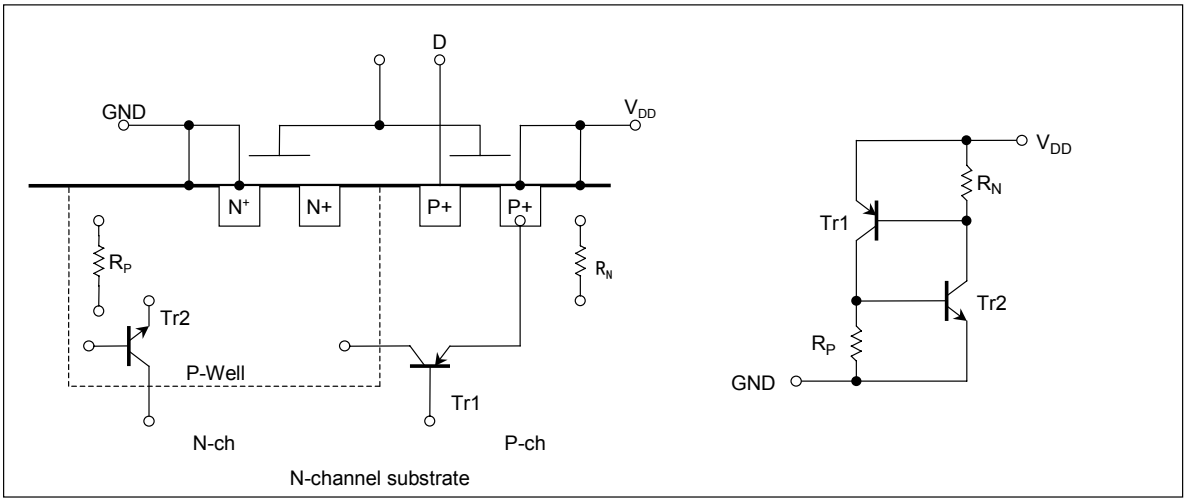


Figure 3.30 Sectional structure of CMOS and equivalent circuit

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